



OK to enter

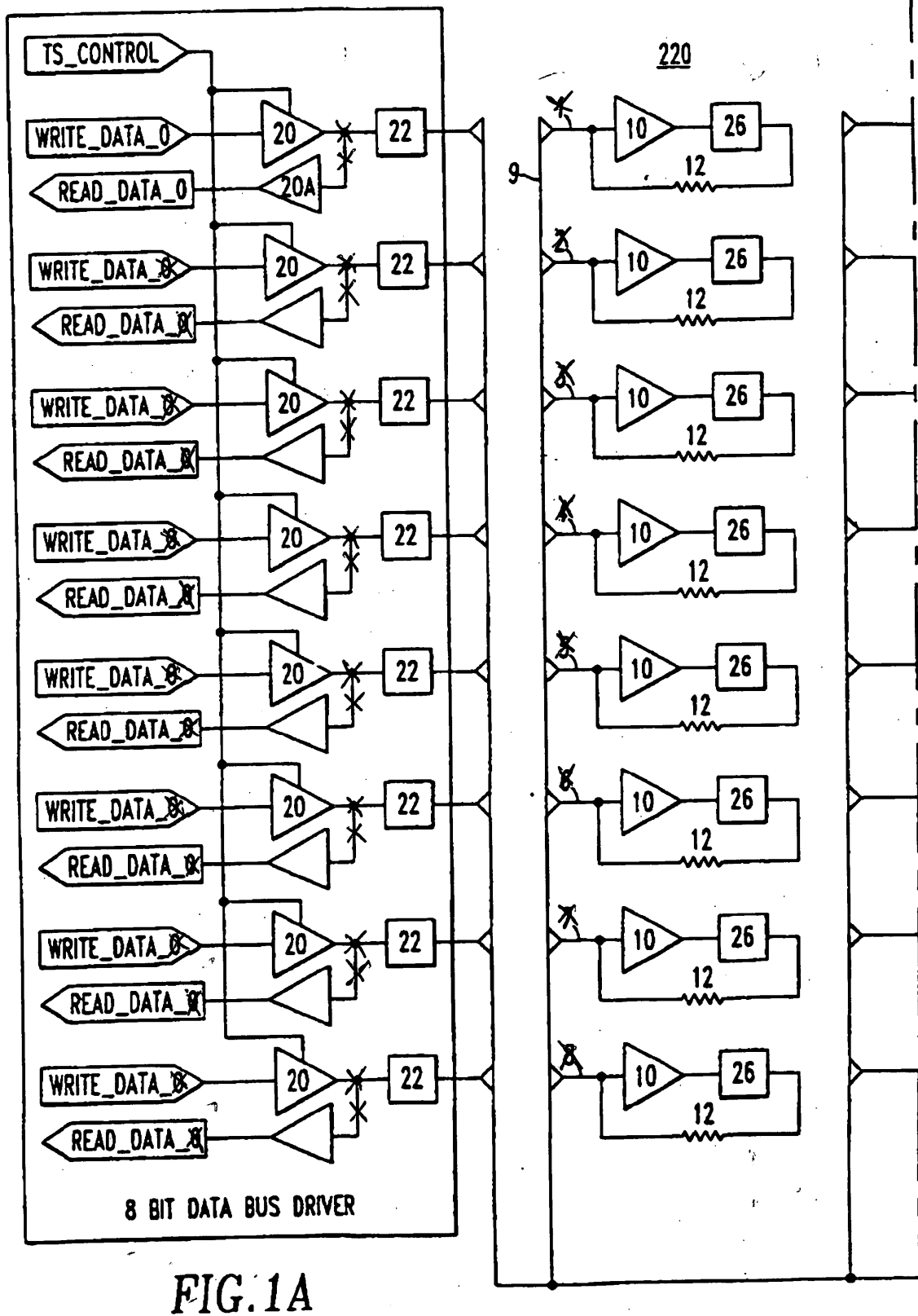


FIG. 1A

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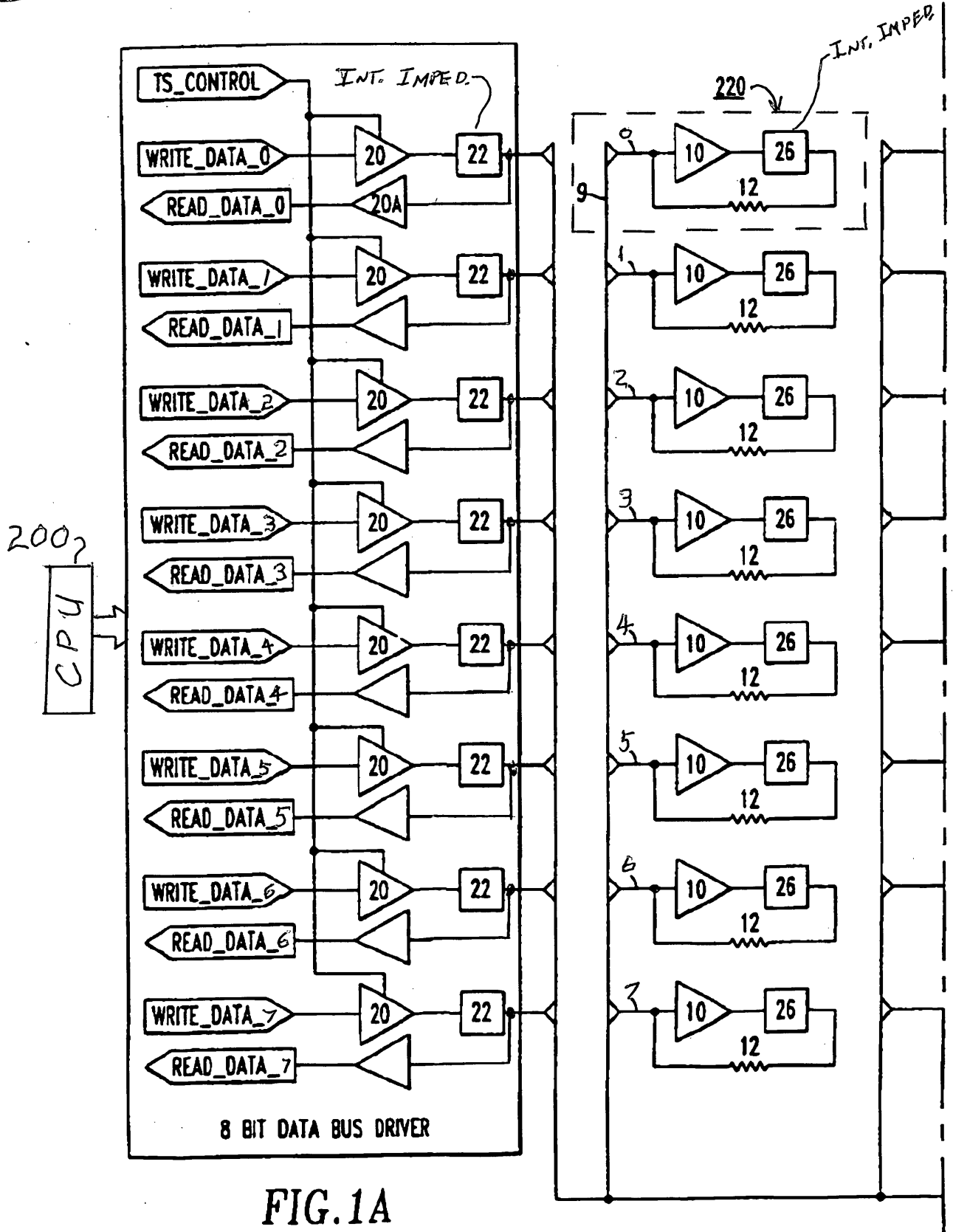
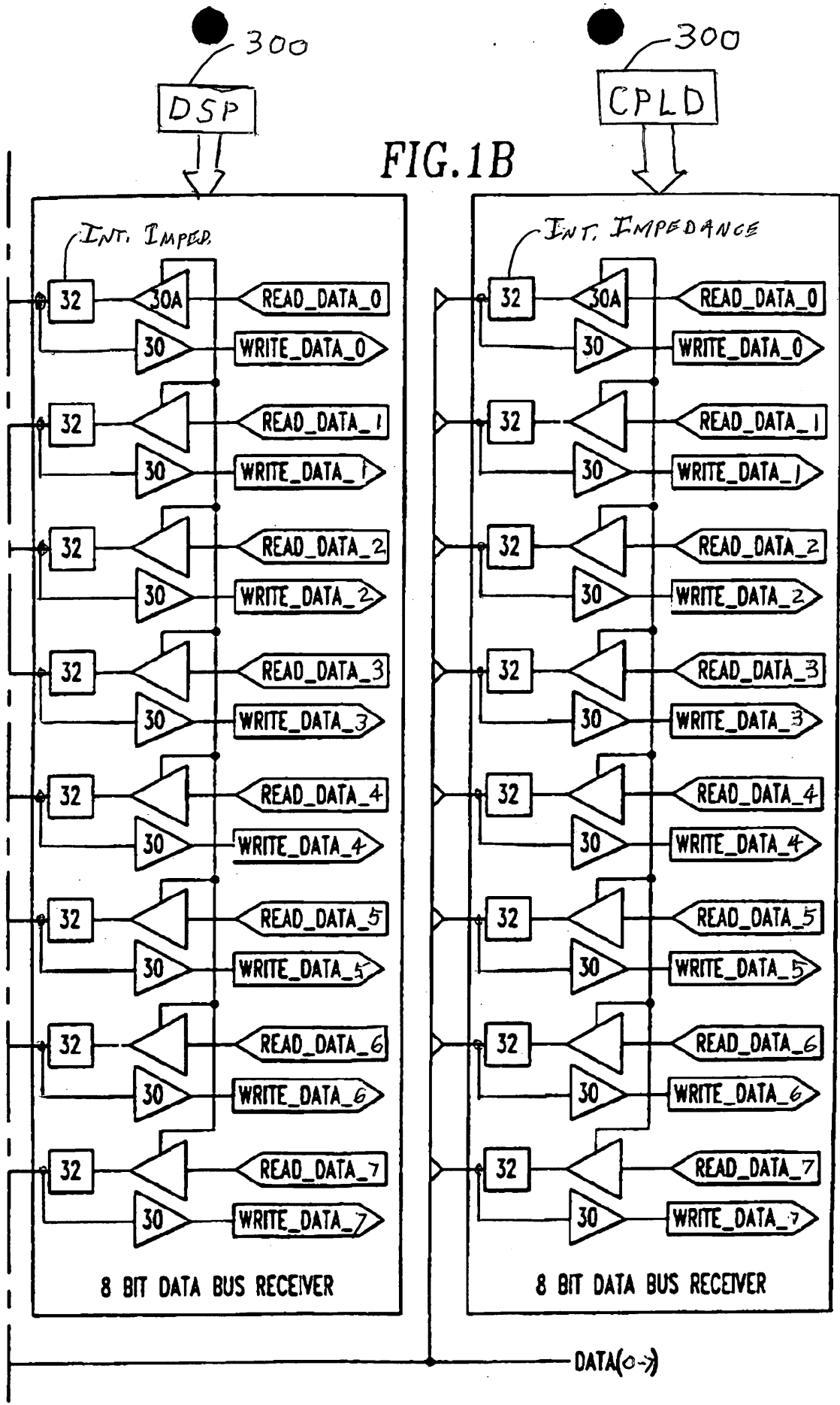


FIG. 1A

FIG. 1B



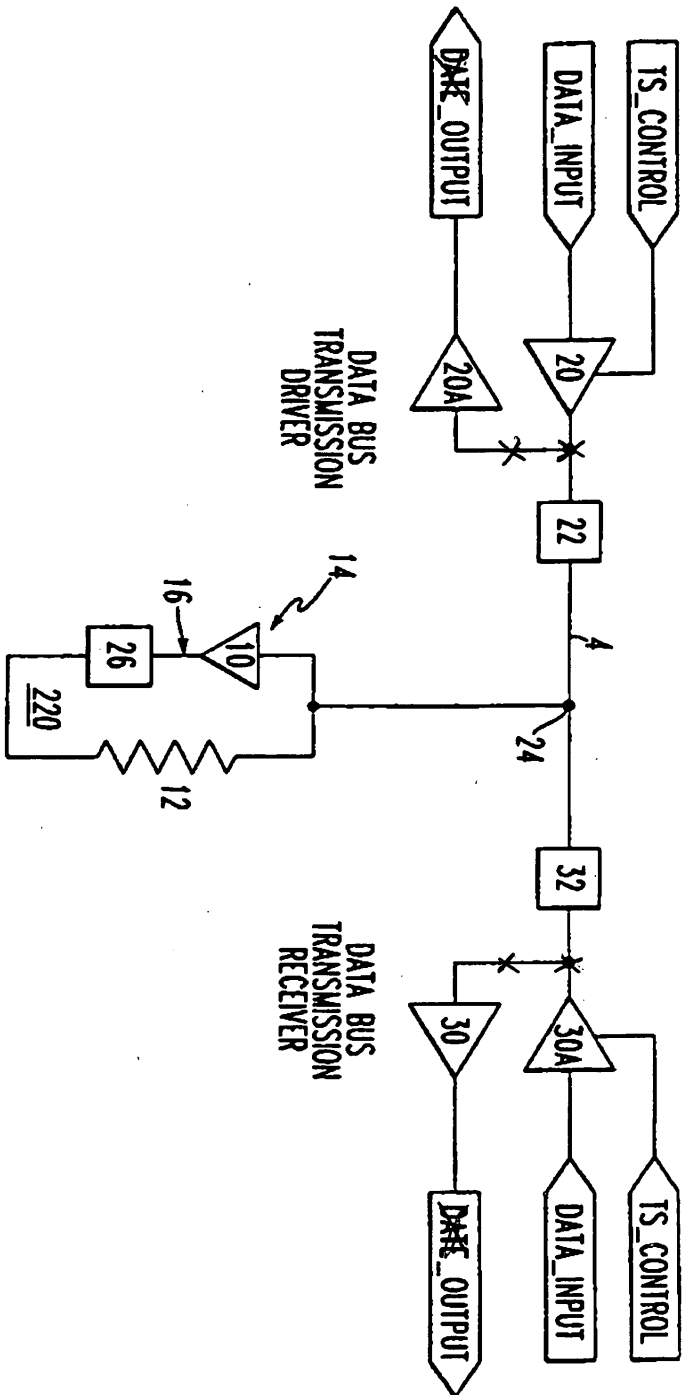


FIG. 2

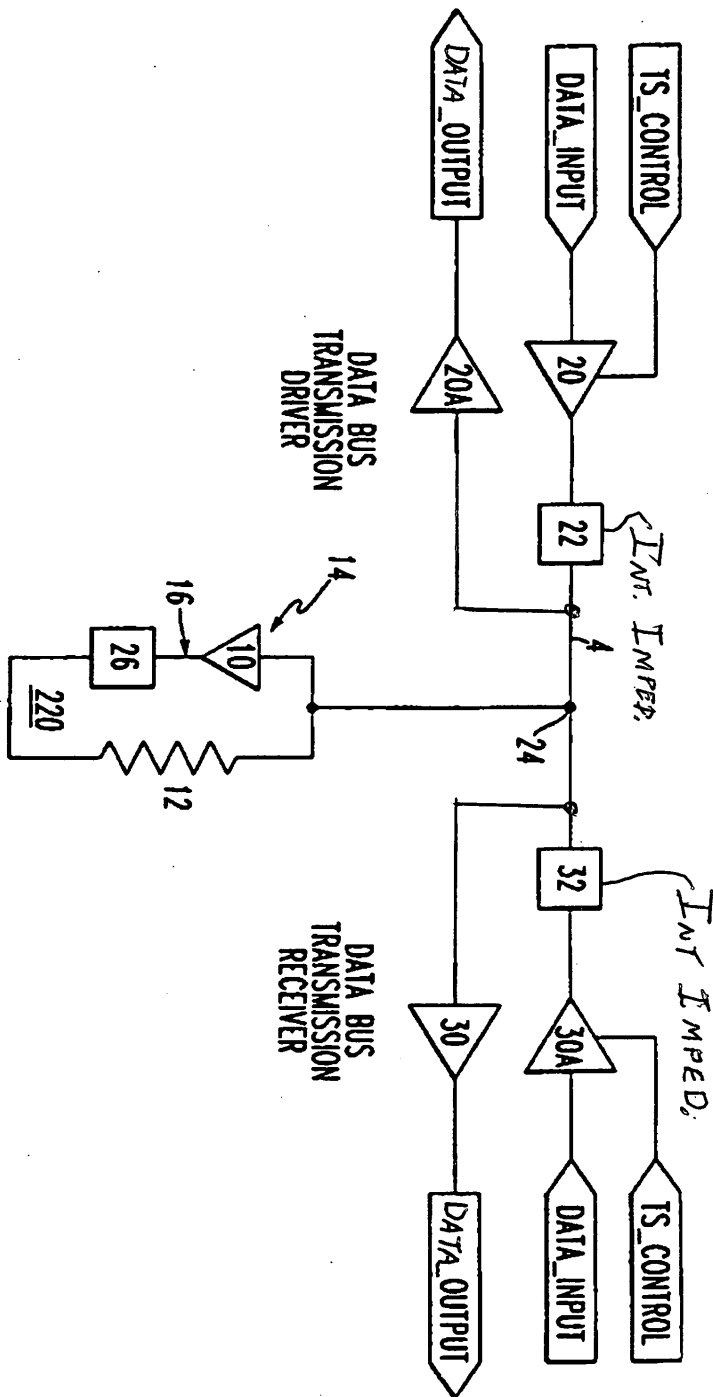
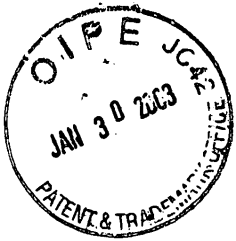
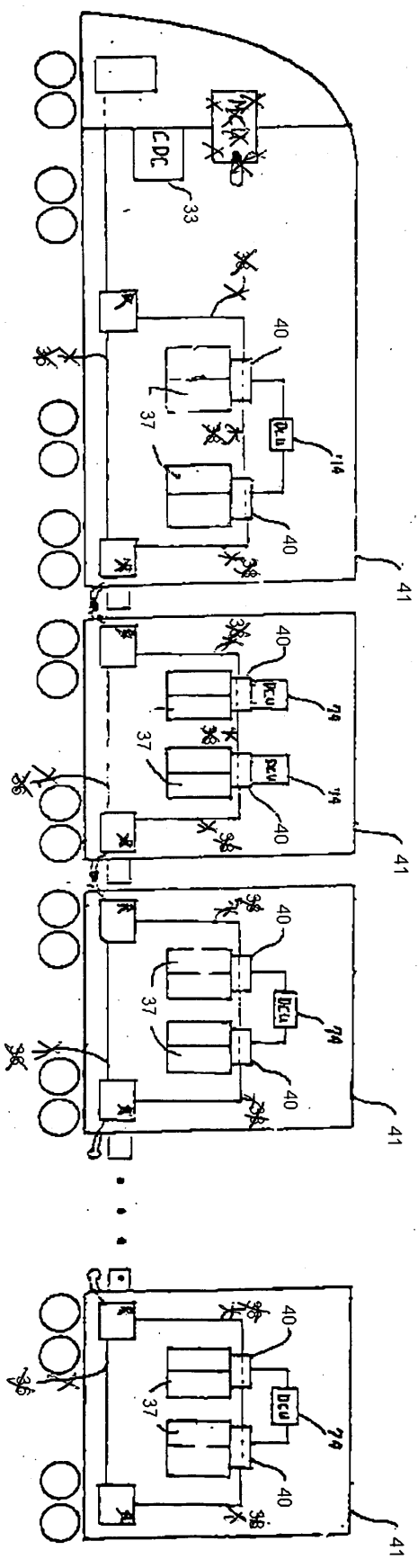
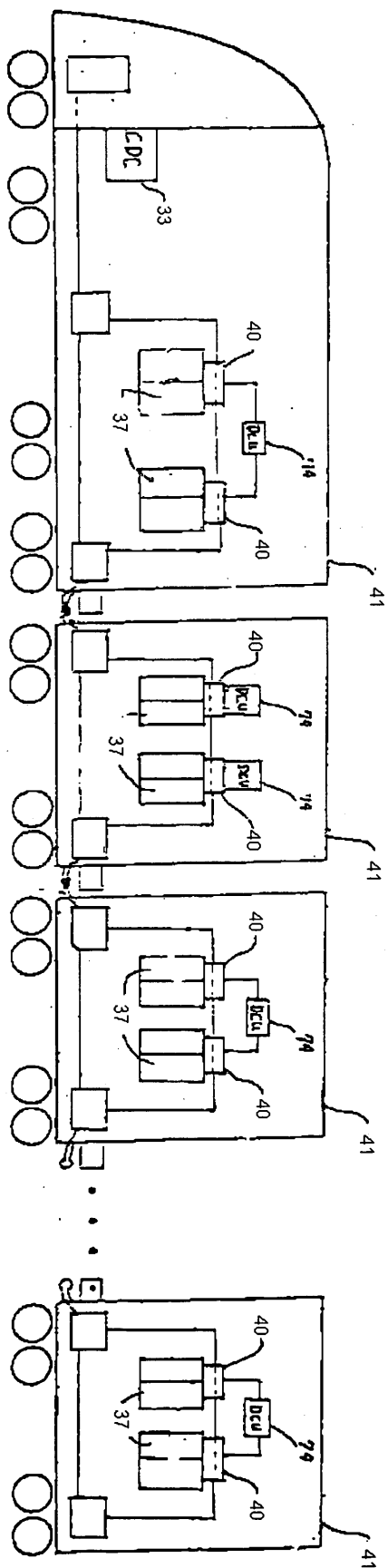
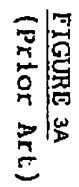


FIG.2



FIGURE 3A
(Prior Art)





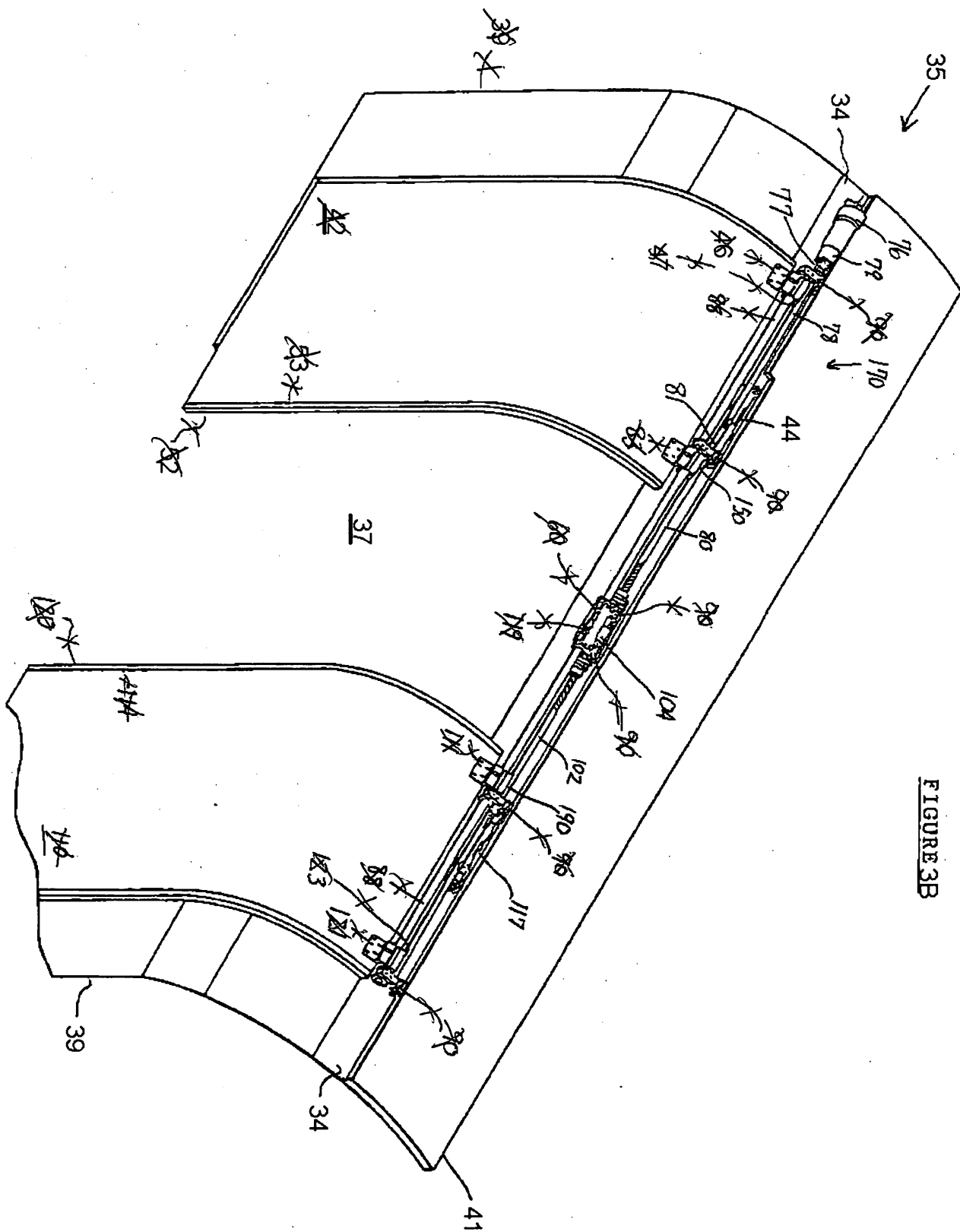


FIGURE 3B

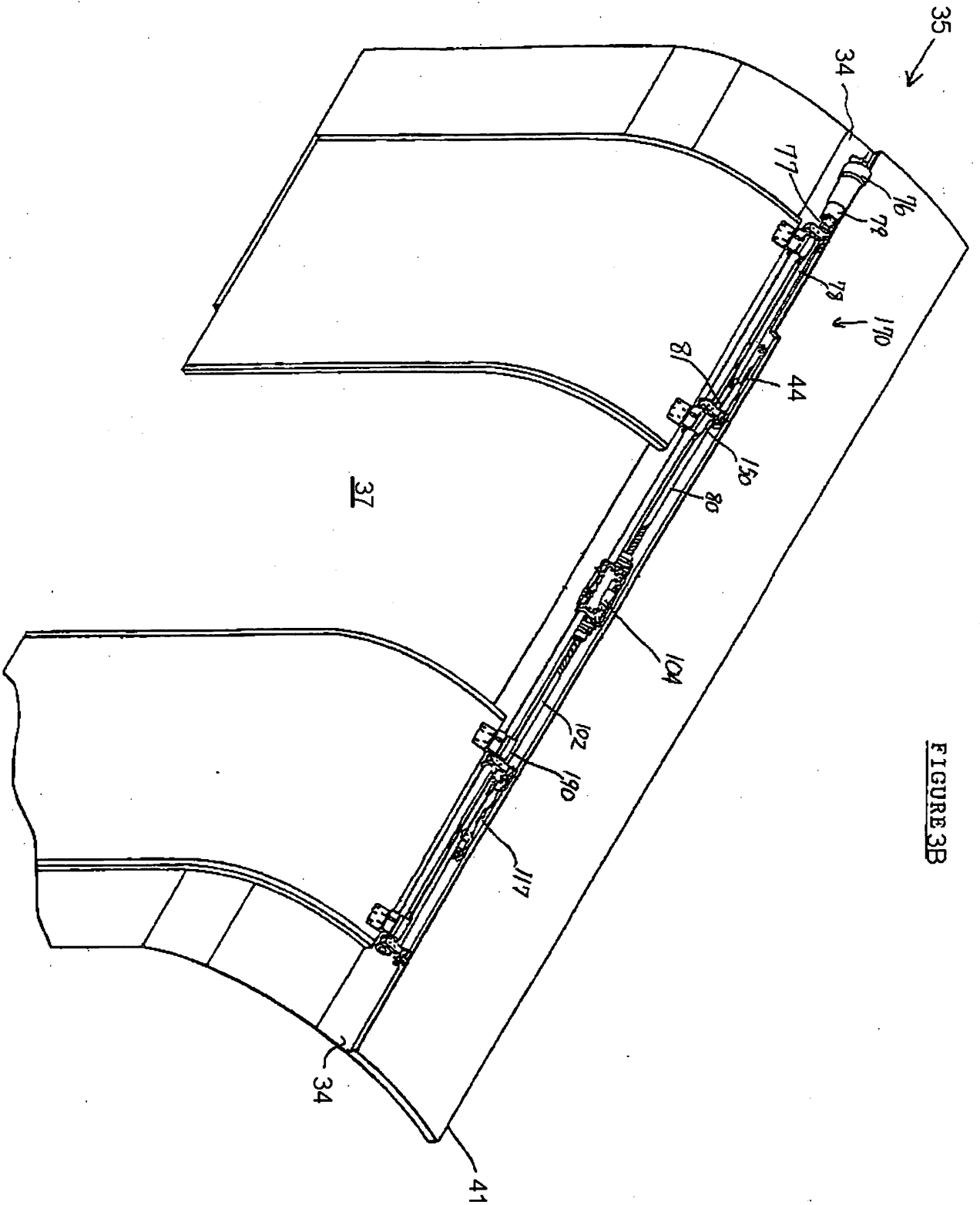
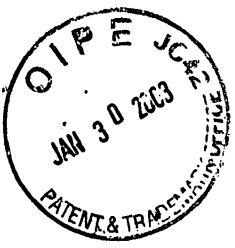


FIGURE 3B

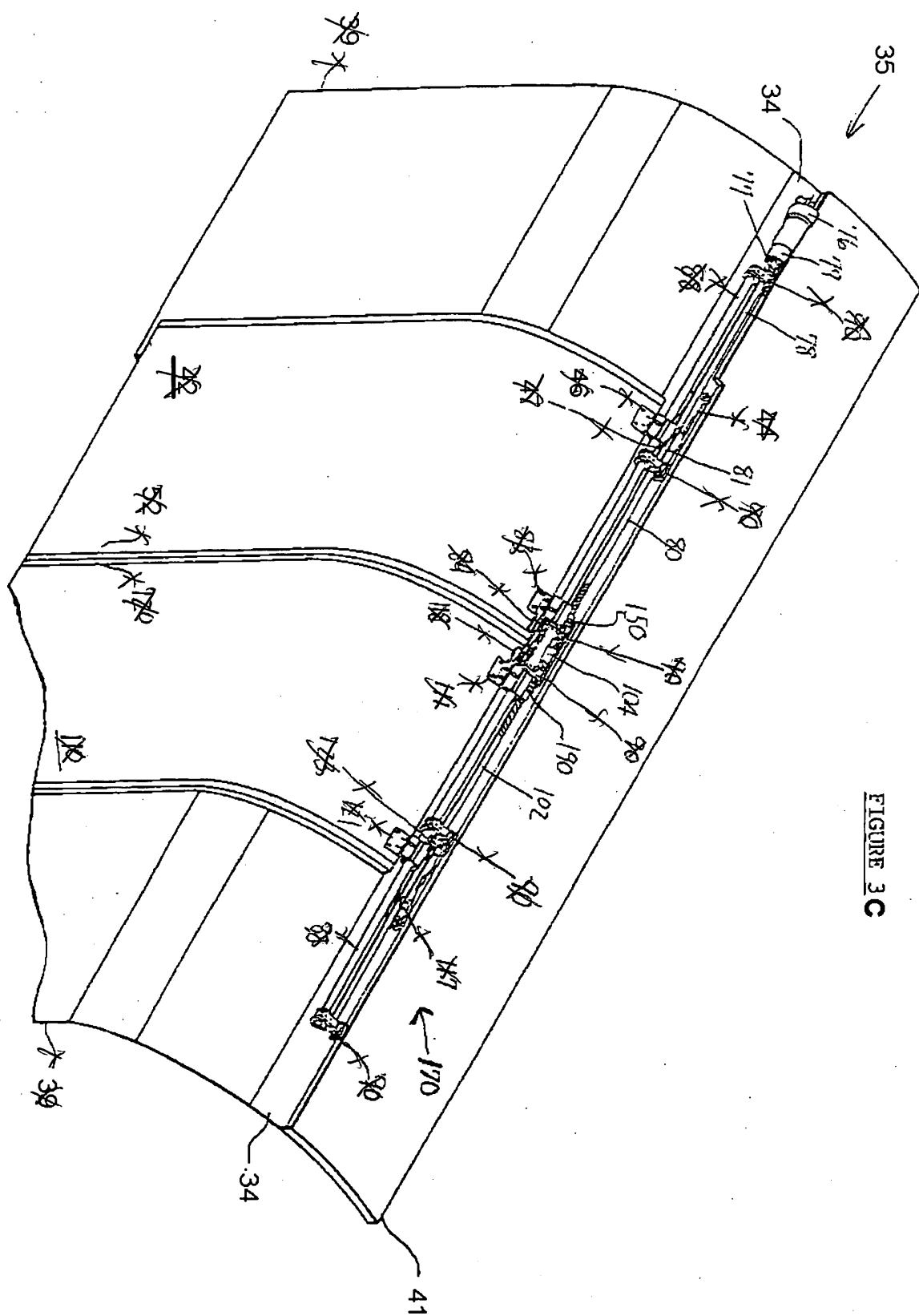


FIGURE 3C

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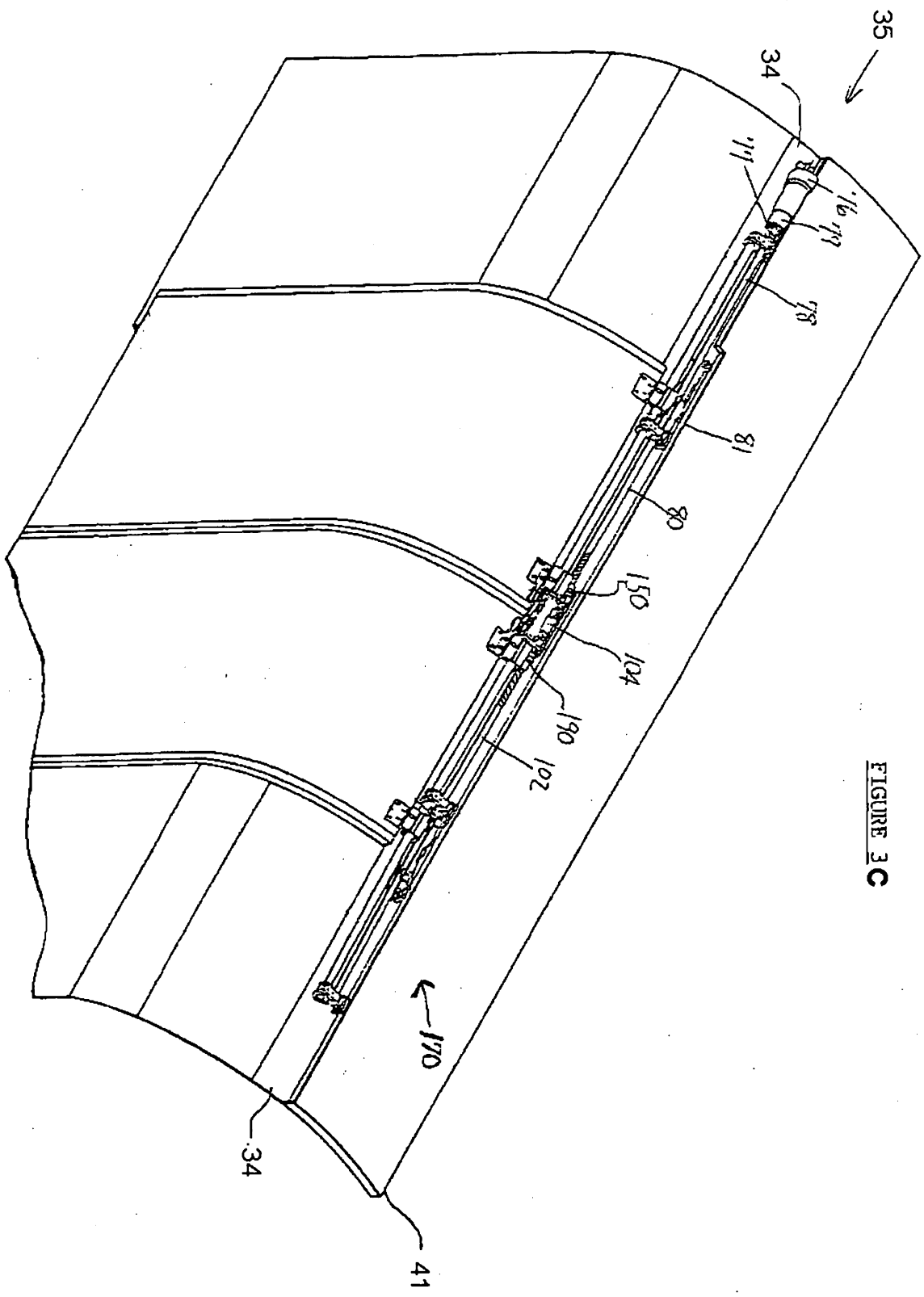
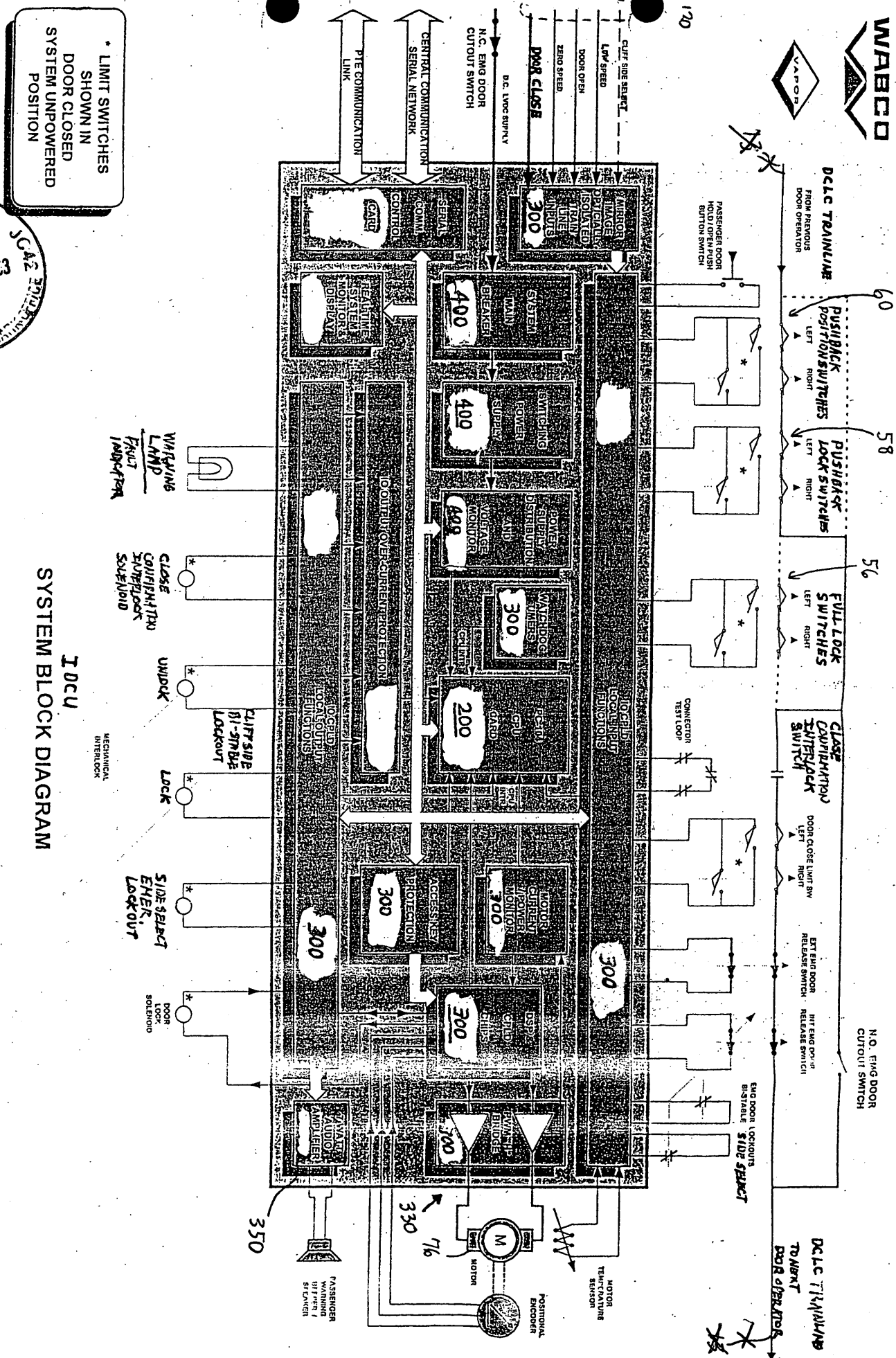


FIGURE 3C





• LIMIT SWITCHES
SHOWN IN
DOOR CLOSED
SYSTEM UNPOWERED
POSITION



FIGURE 7A

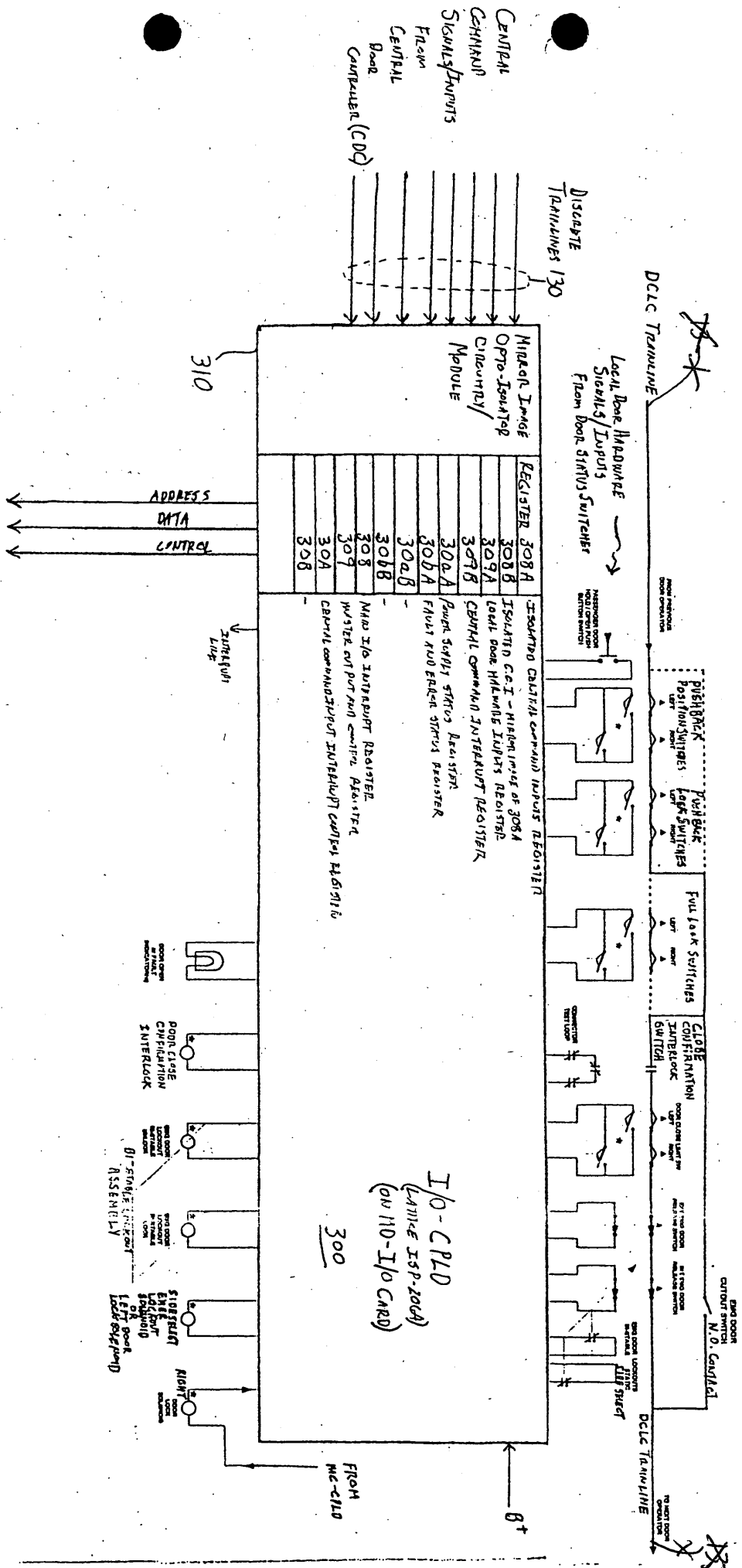


FIGURE 5A

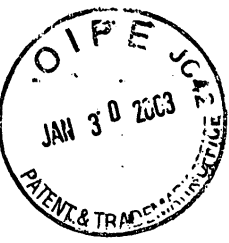
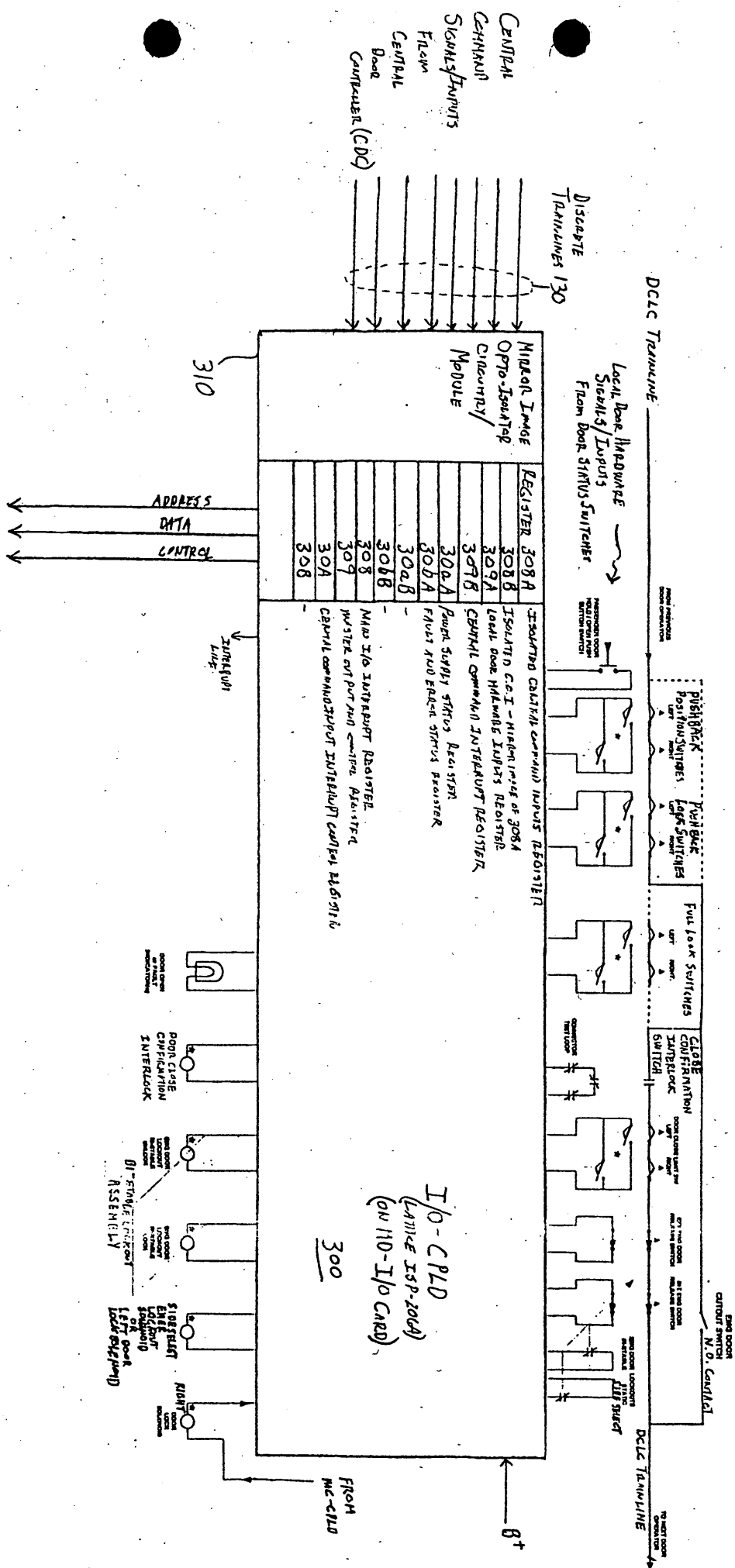




FIGURE 5B

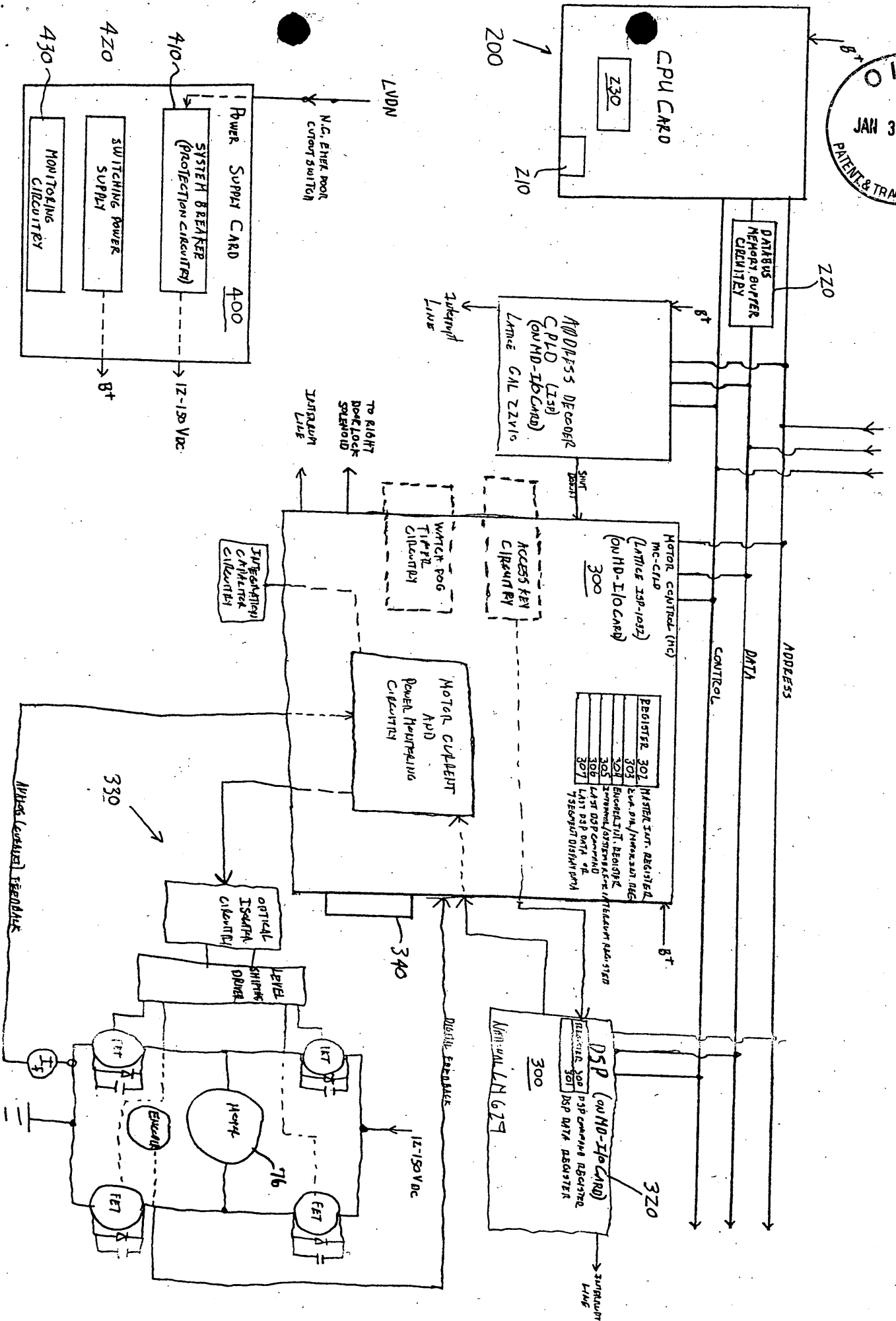




FIGURE 8

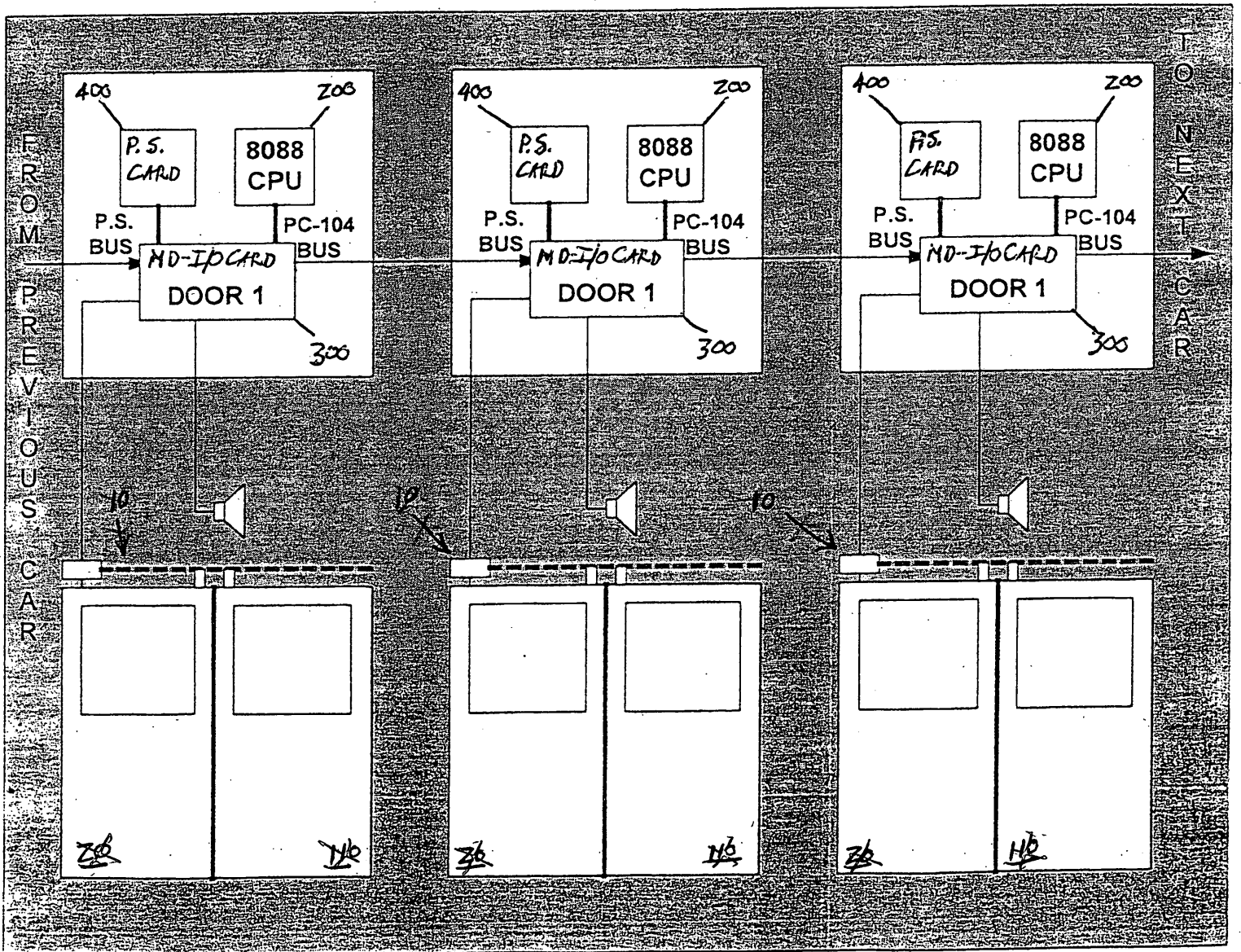




FIGURE 6

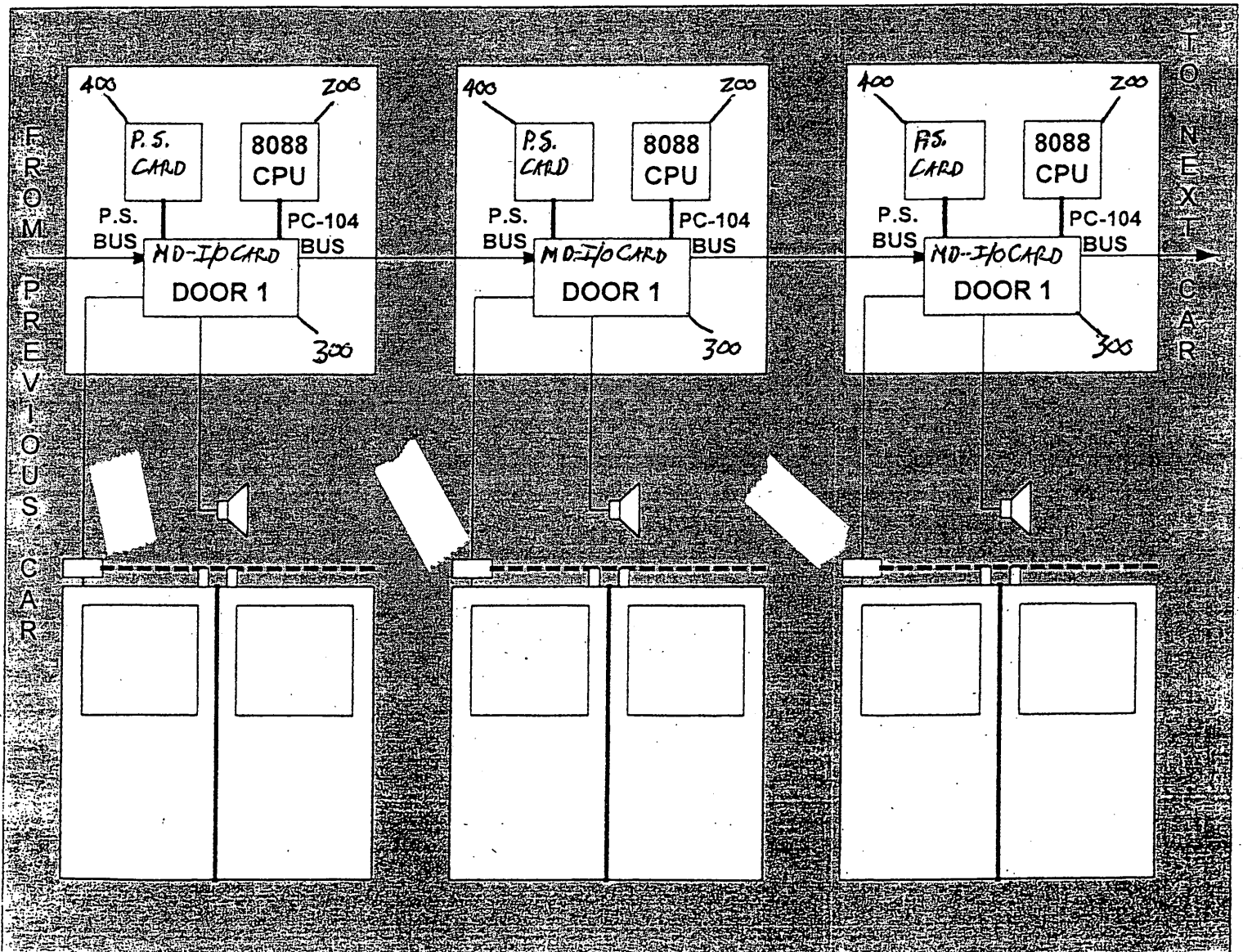


FIGURE 3

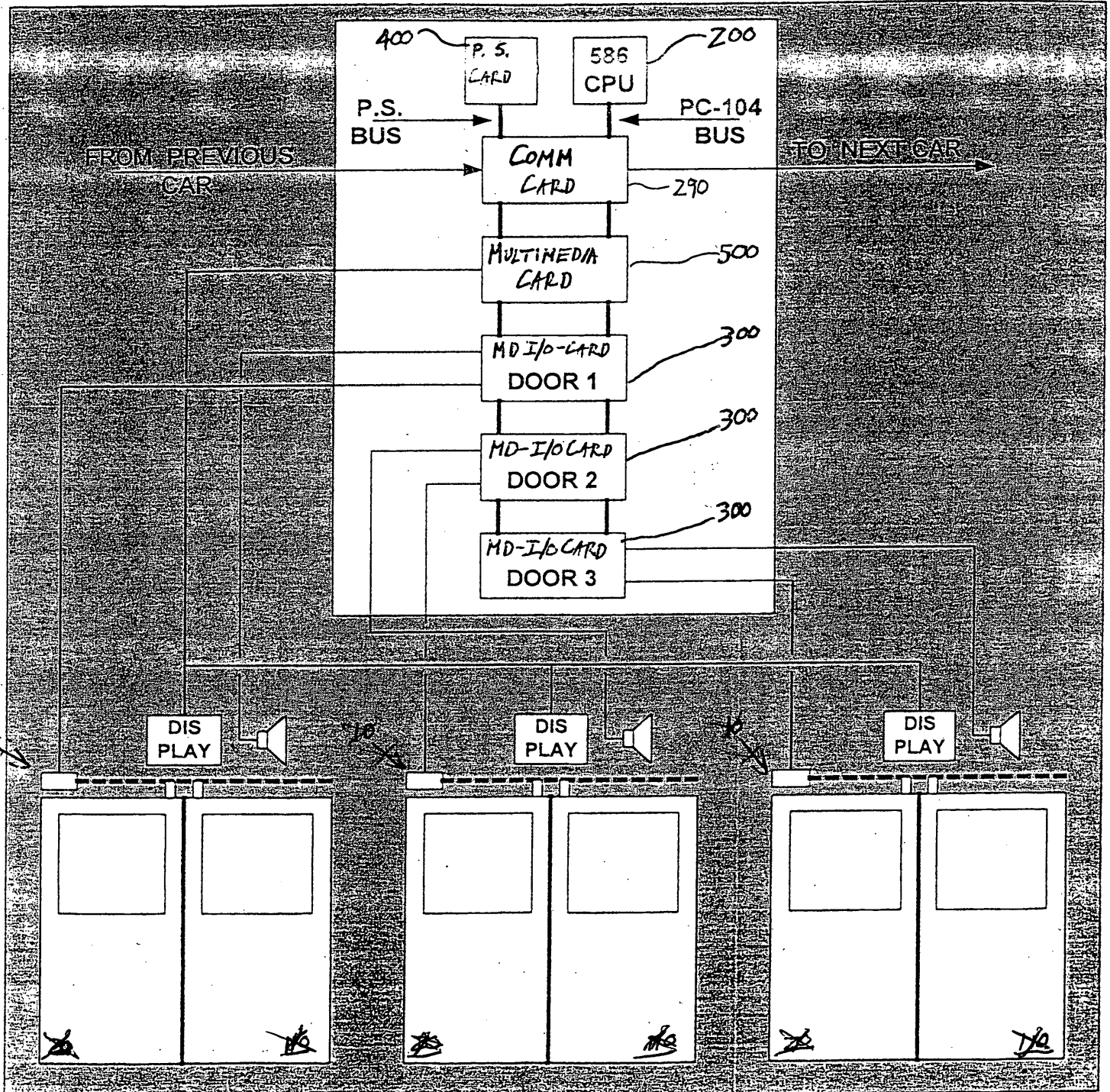
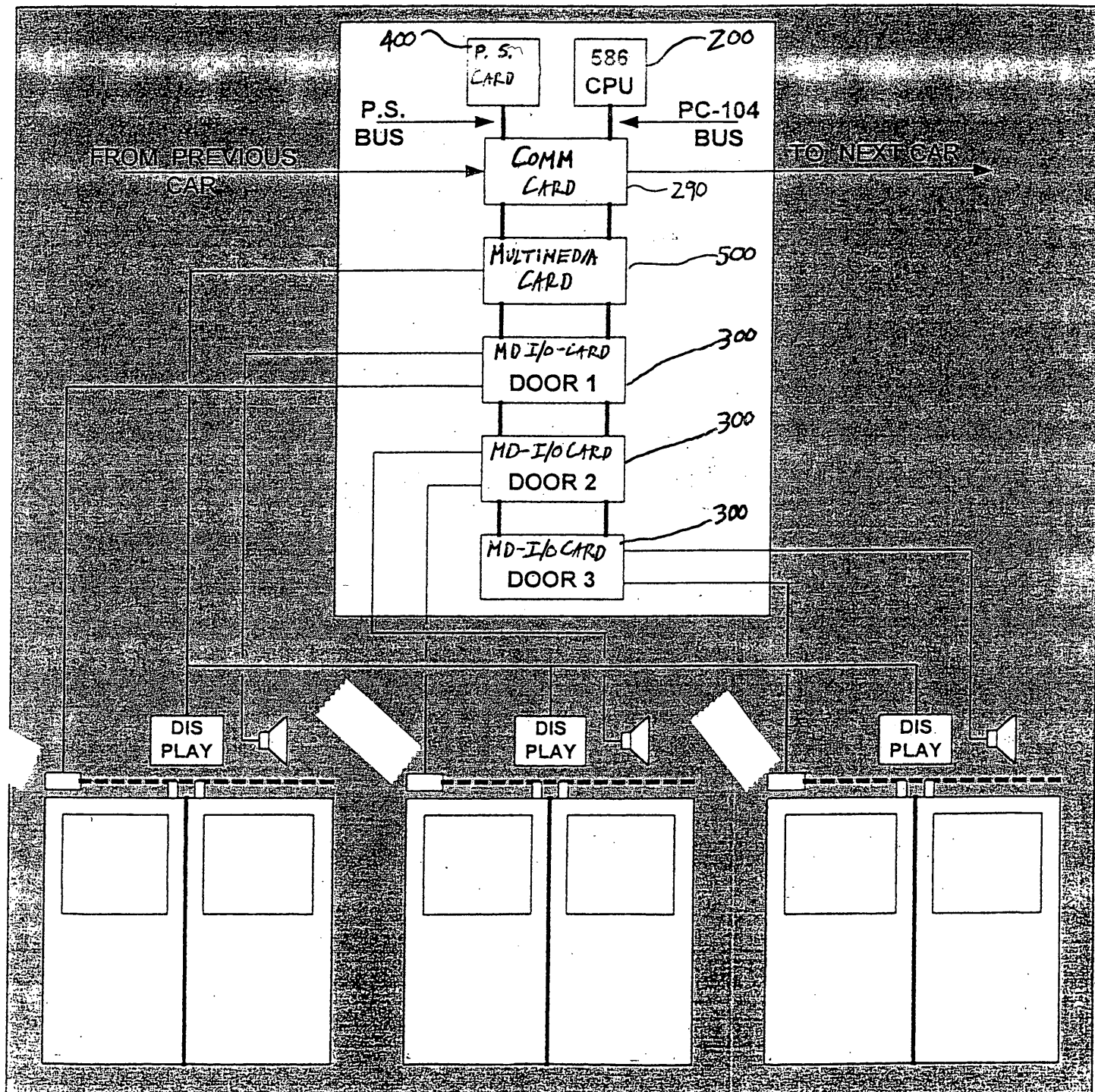
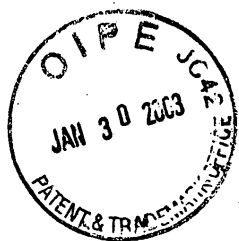


FIGURE 7

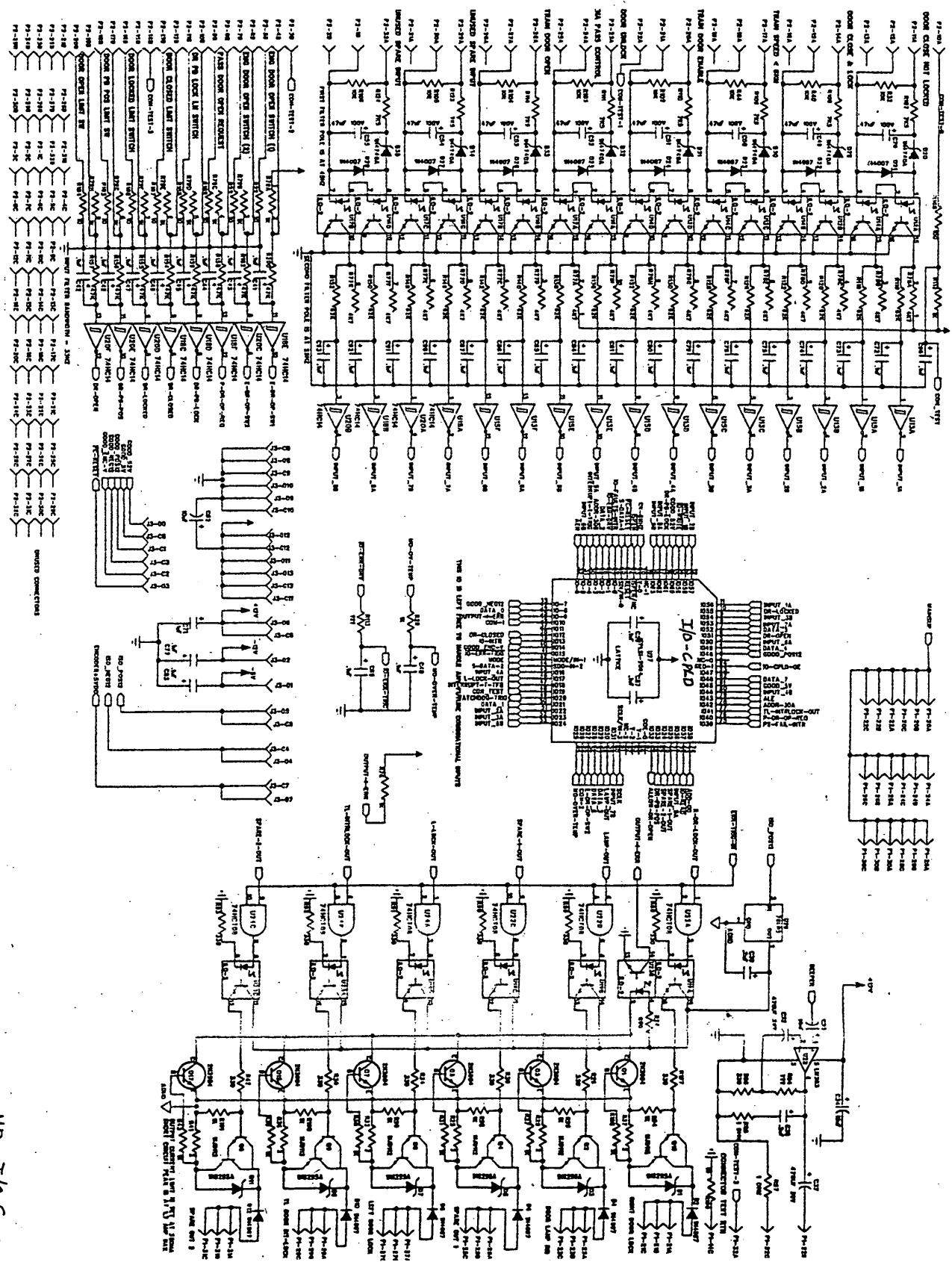




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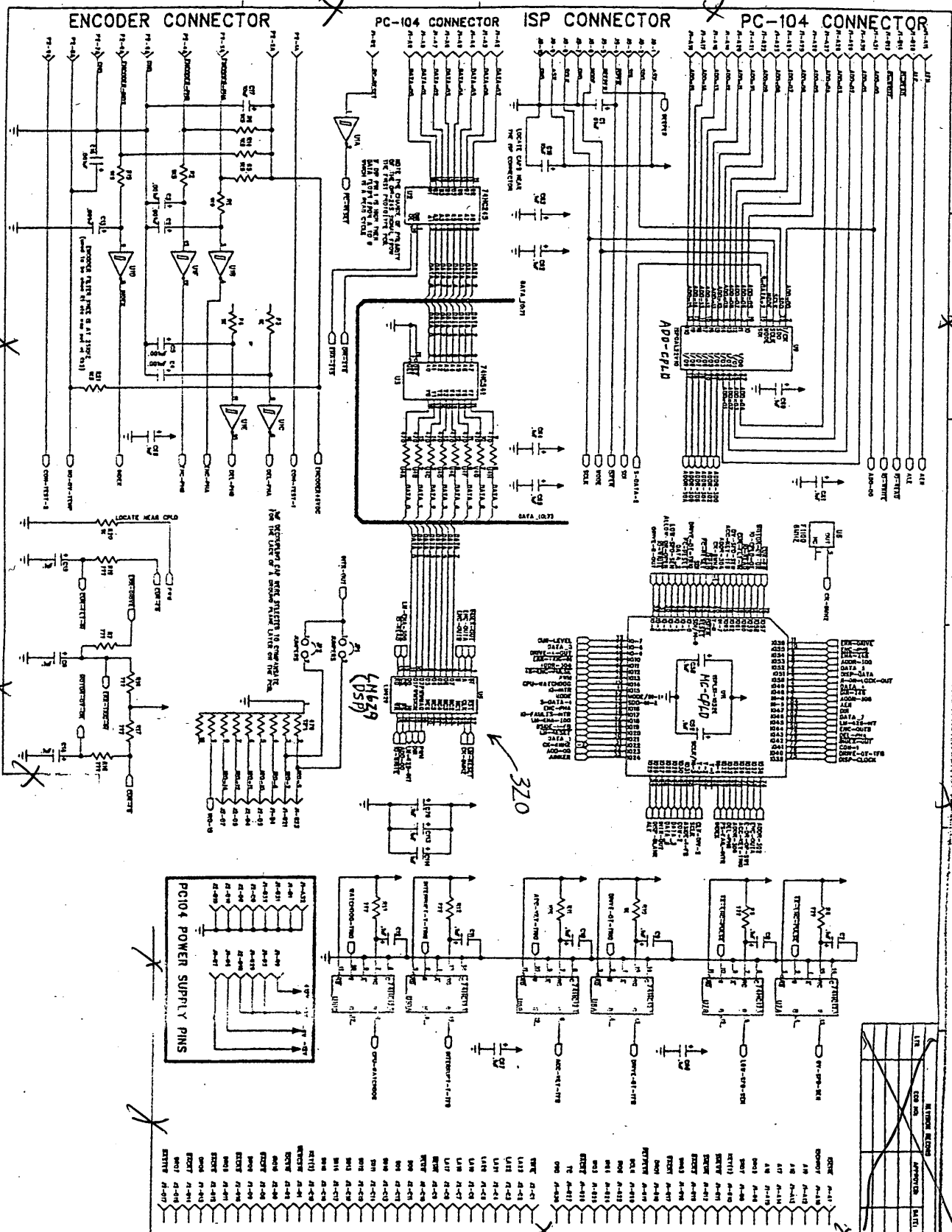
310

FIGURE 8A



MD-I/O CARD
LAYOUT 1

FIGURE 10B



MD-I/O CARD
LAYOUT

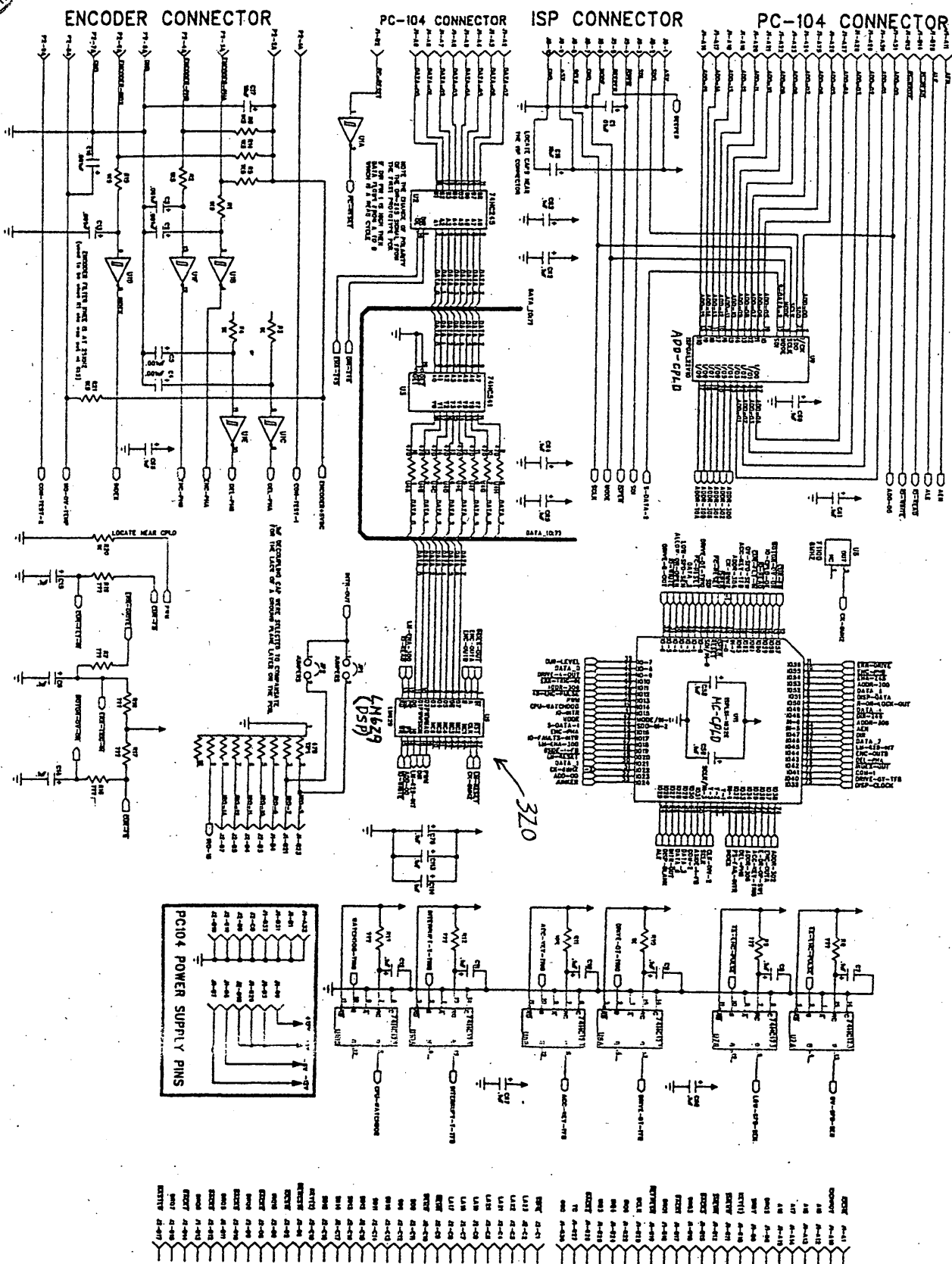
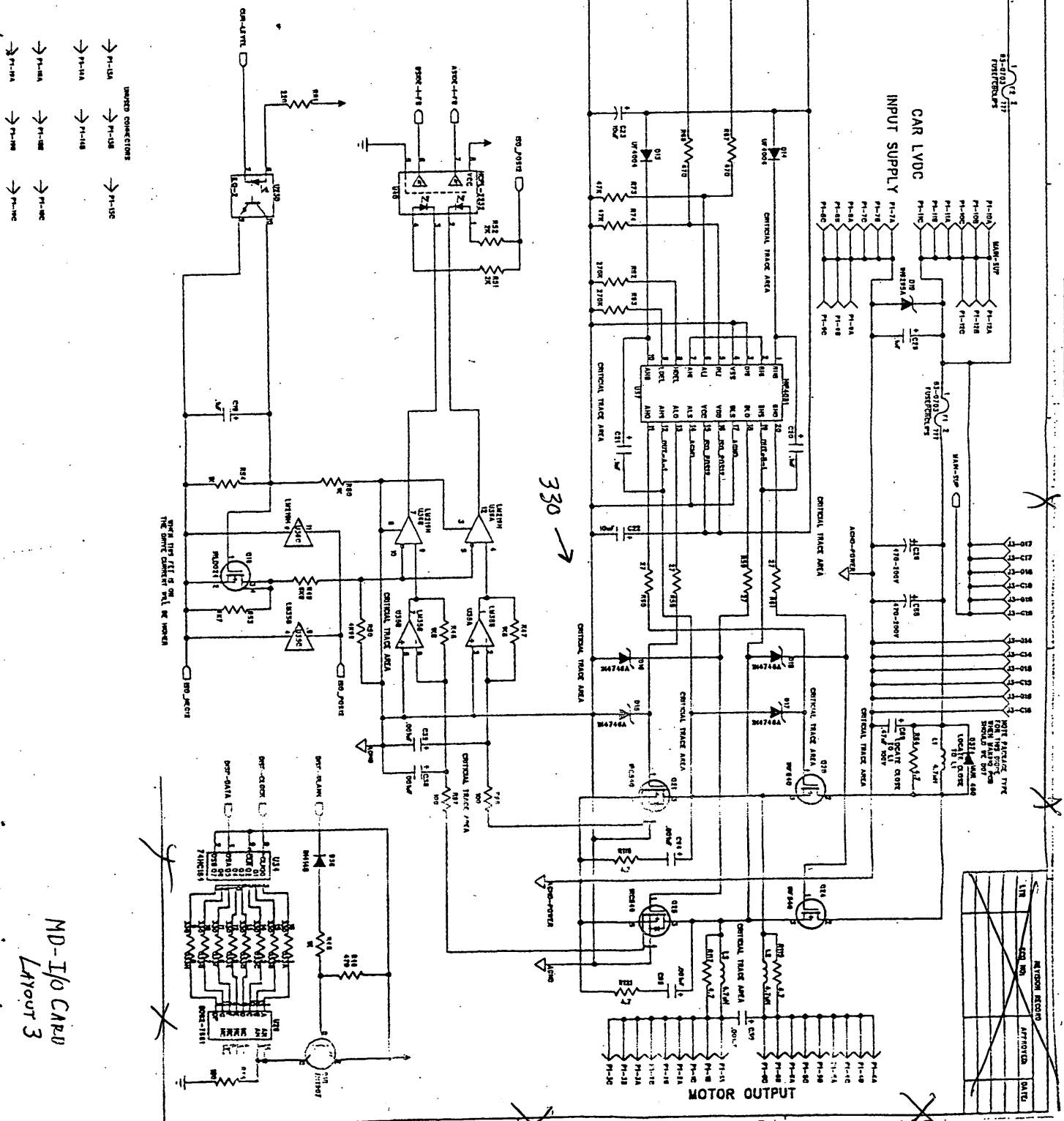


FIGURE 8 B

MD-IPb Card
Layout Z

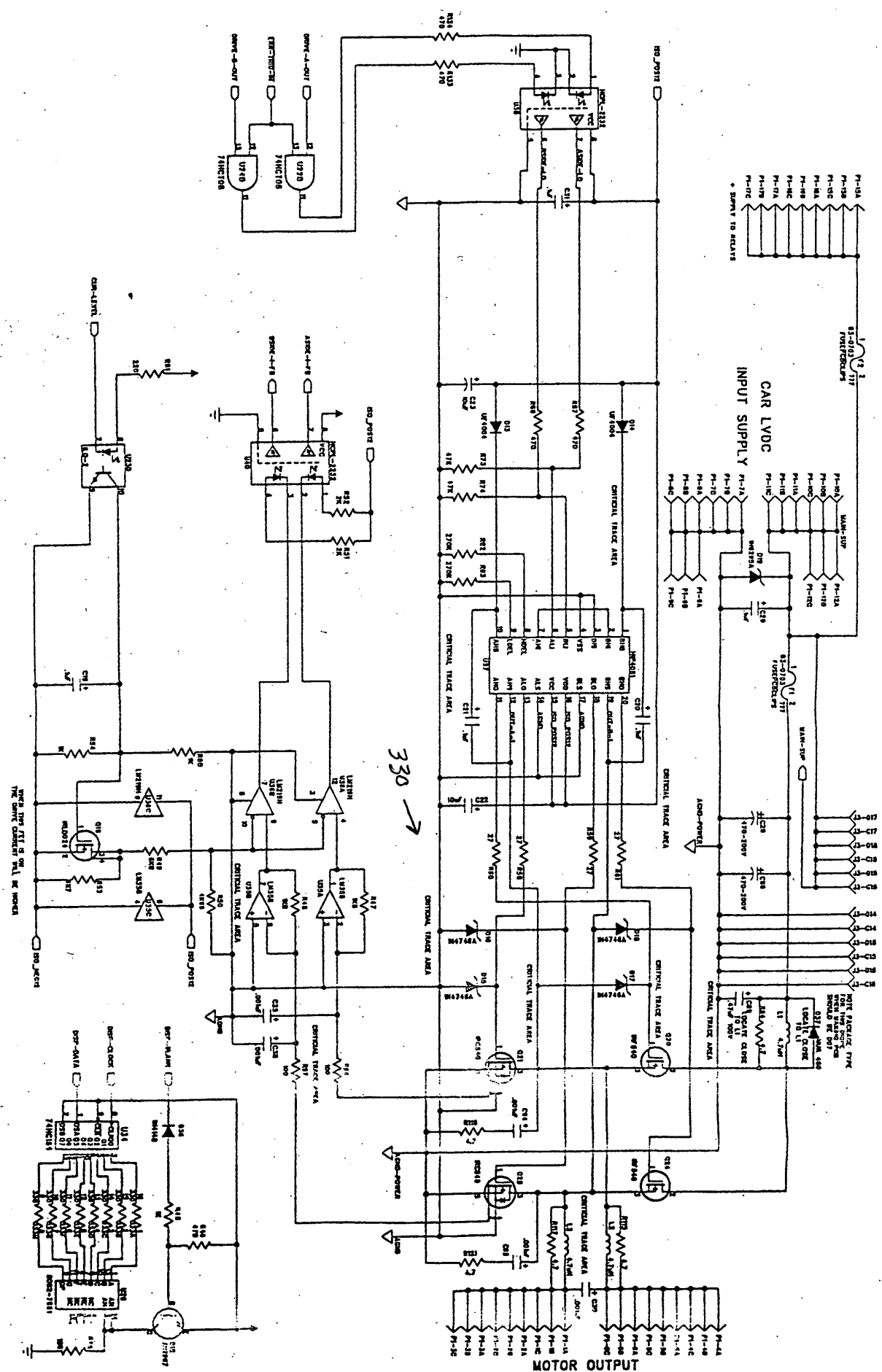
FIGURE 20C



MD-I/O CARU
Layout 3



FIGURE 8 C



UNUSED CONNECTIONS

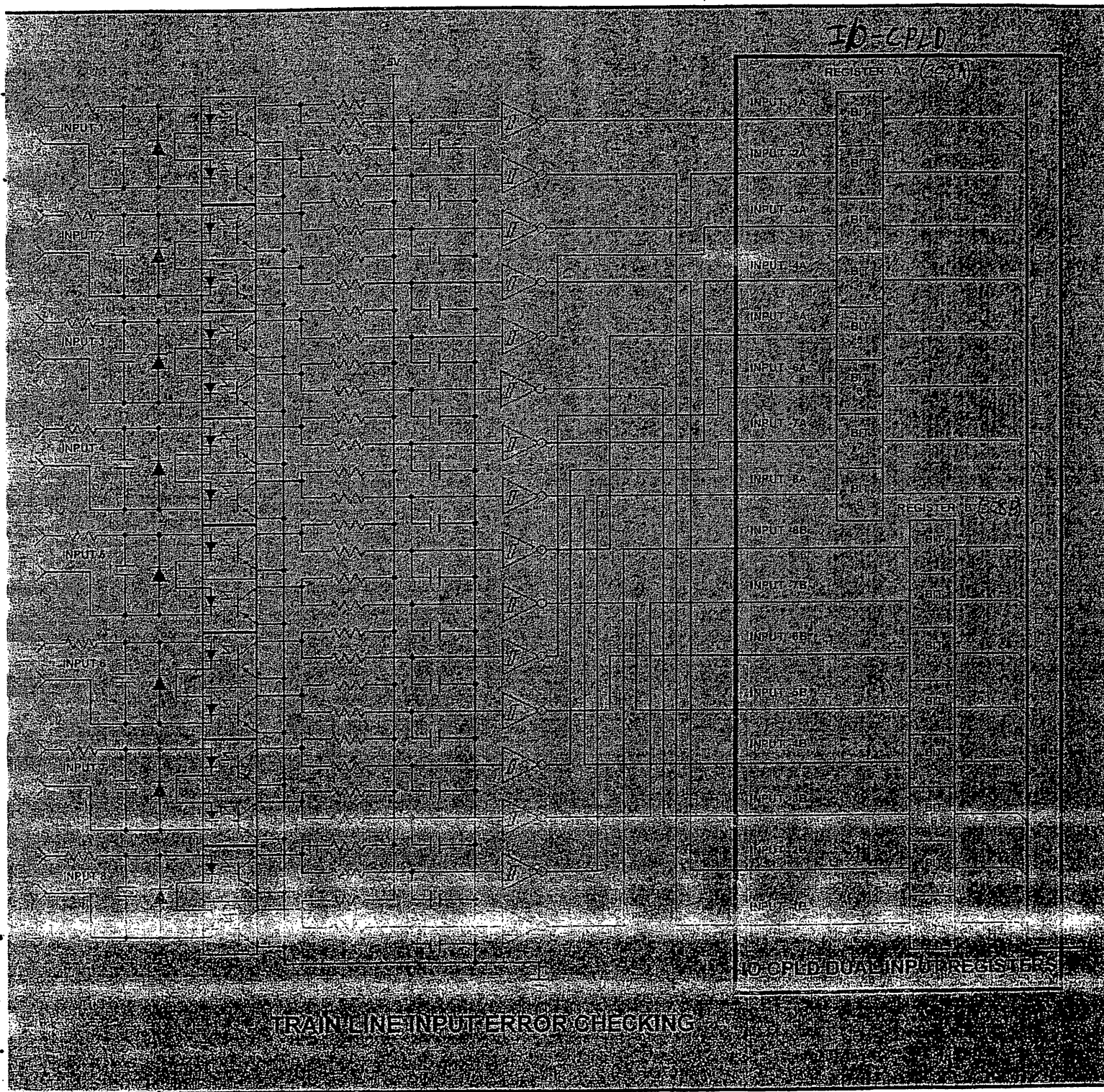
- P1-1A → P1-1B
- P1-1C → P1-1D
- P1-1E → P1-1F
- P1-1G → P1-1H
- P1-1I → P1-1J
- P1-1K → P1-1L
- P1-1M → P1-1N
- P1-1O → P1-1P
- P1-1Q → P1-1R
- P1-1S → P1-1T
- P1-1U → P1-1V
- P1-1W → P1-1X
- P1-1Y → P1-1Z

MD-I/O CARD
Layout 3



FIGURE ~~A~~

310



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FIGURE 9

310

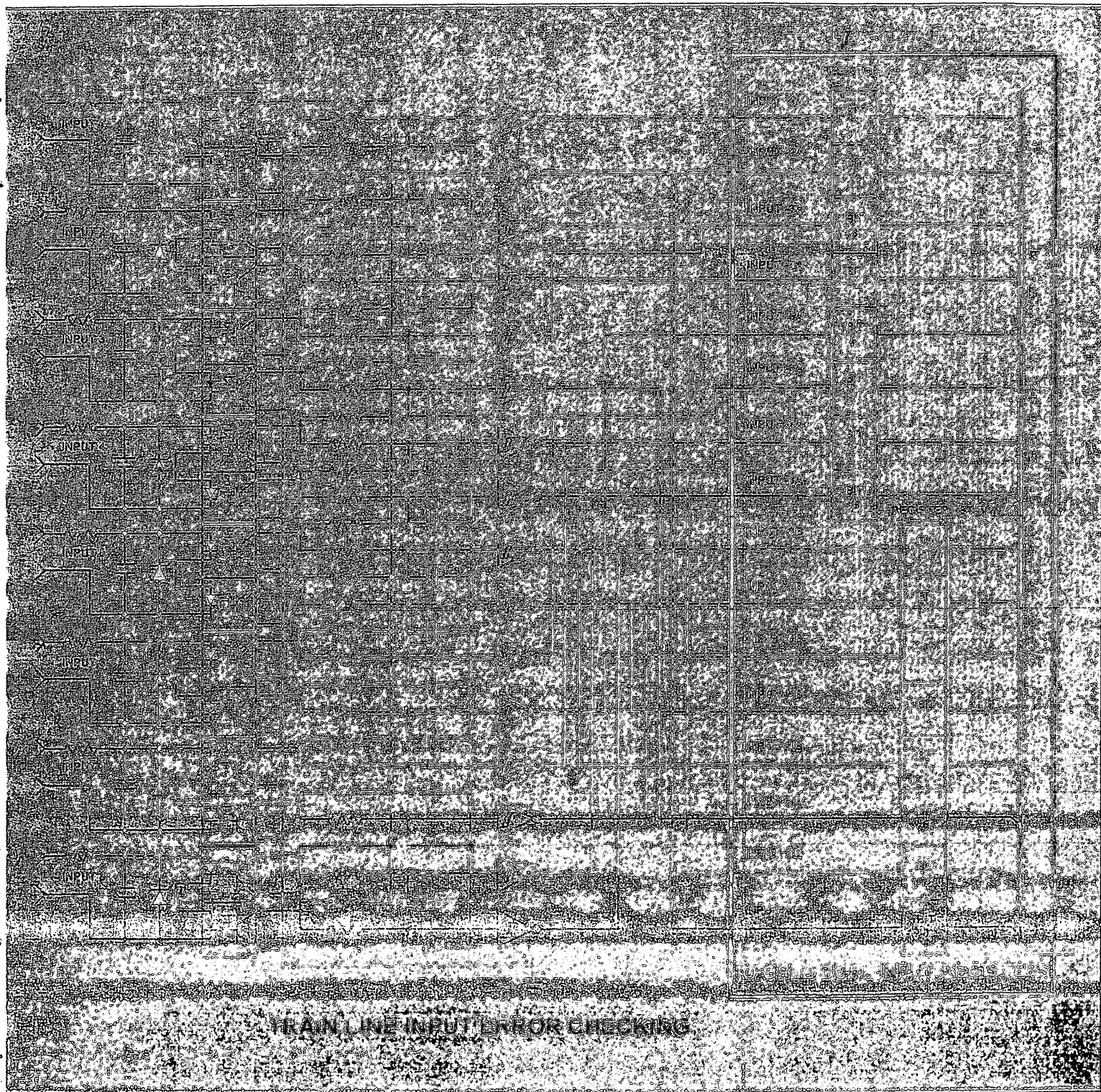
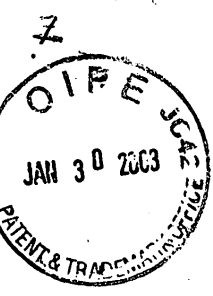
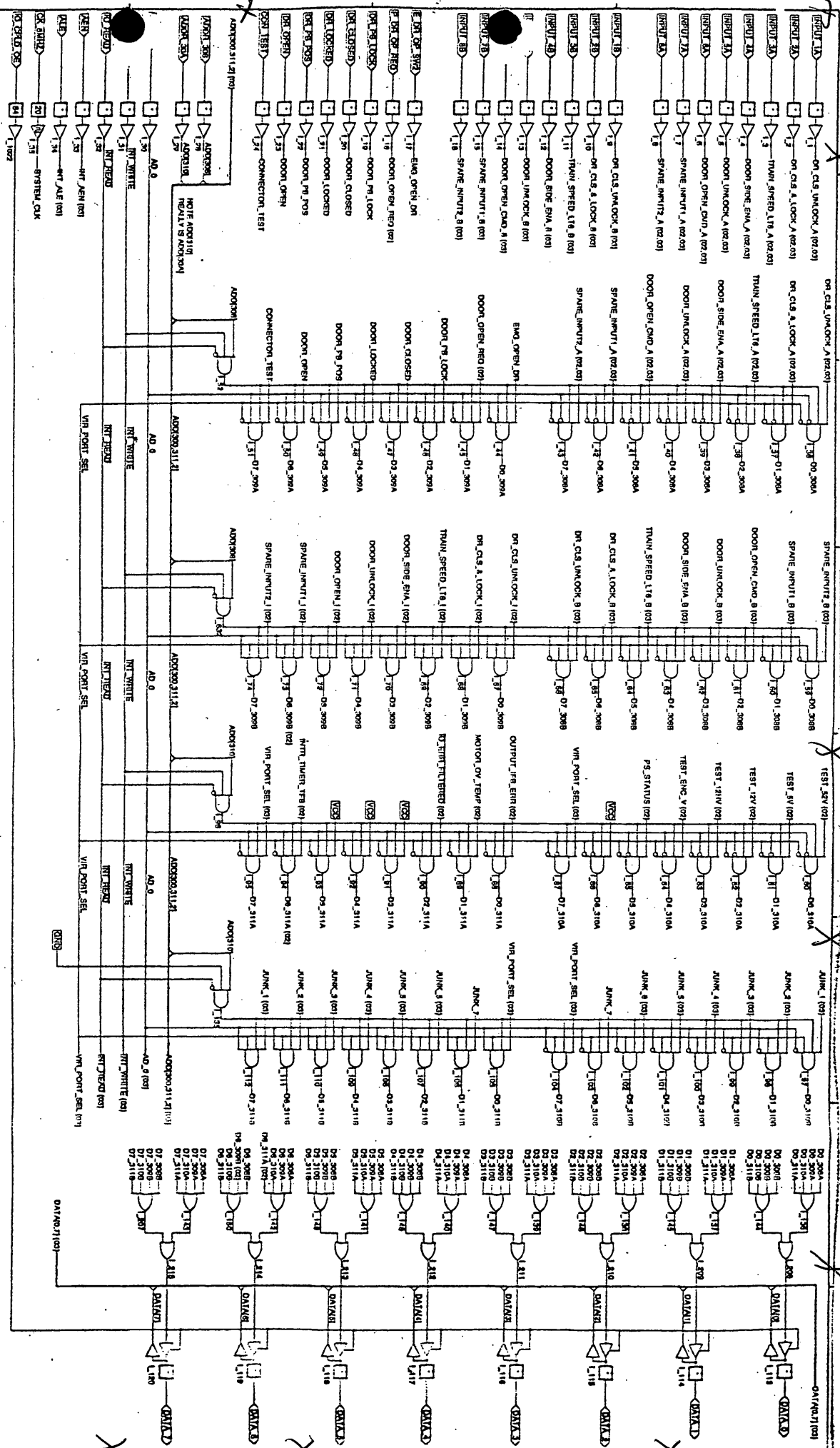
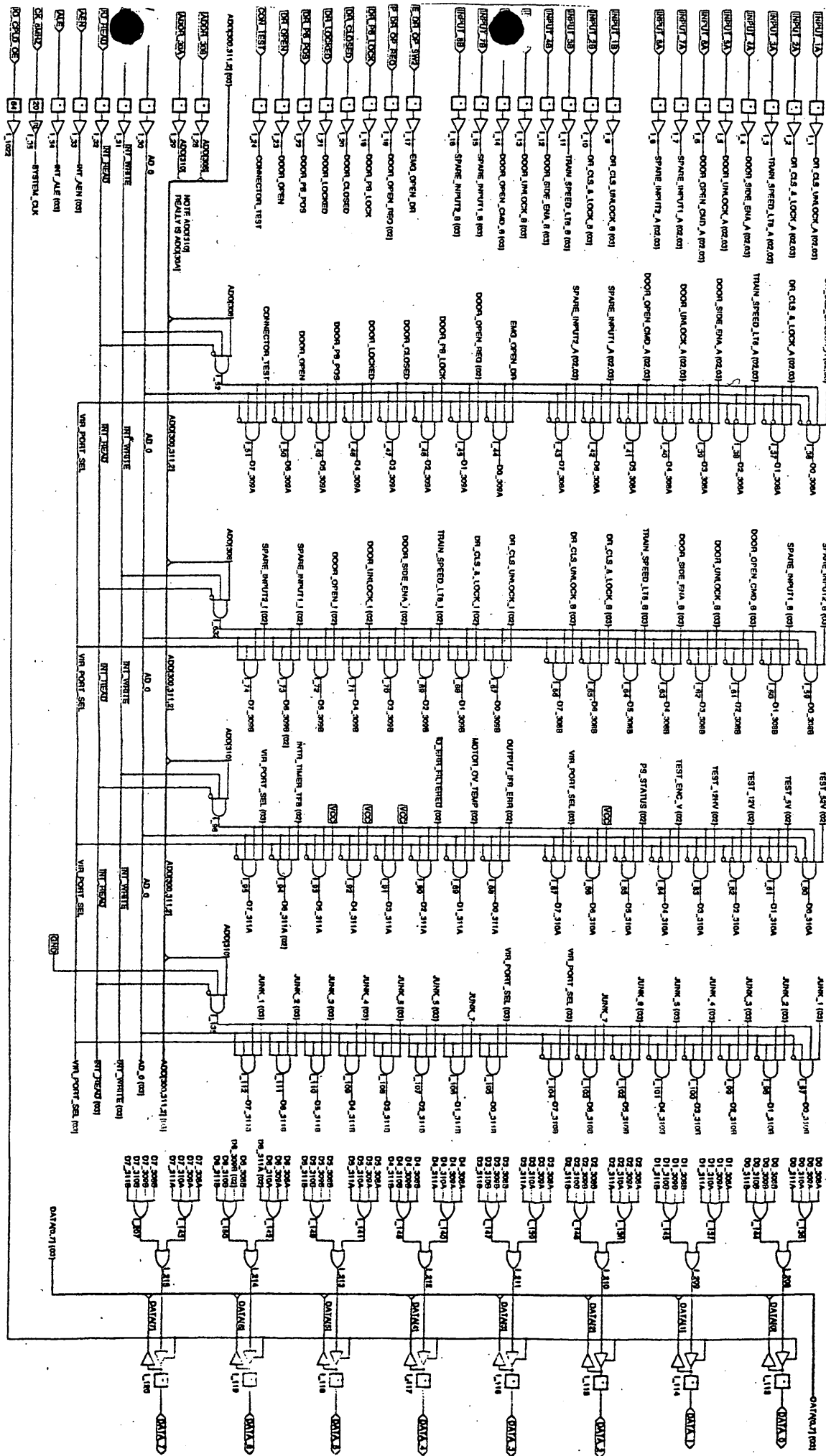


FIGURE 1A



MD-I/O CARD
(I/O-CARD DATA/ADDRESS)
CONTROL LOGIC



1000

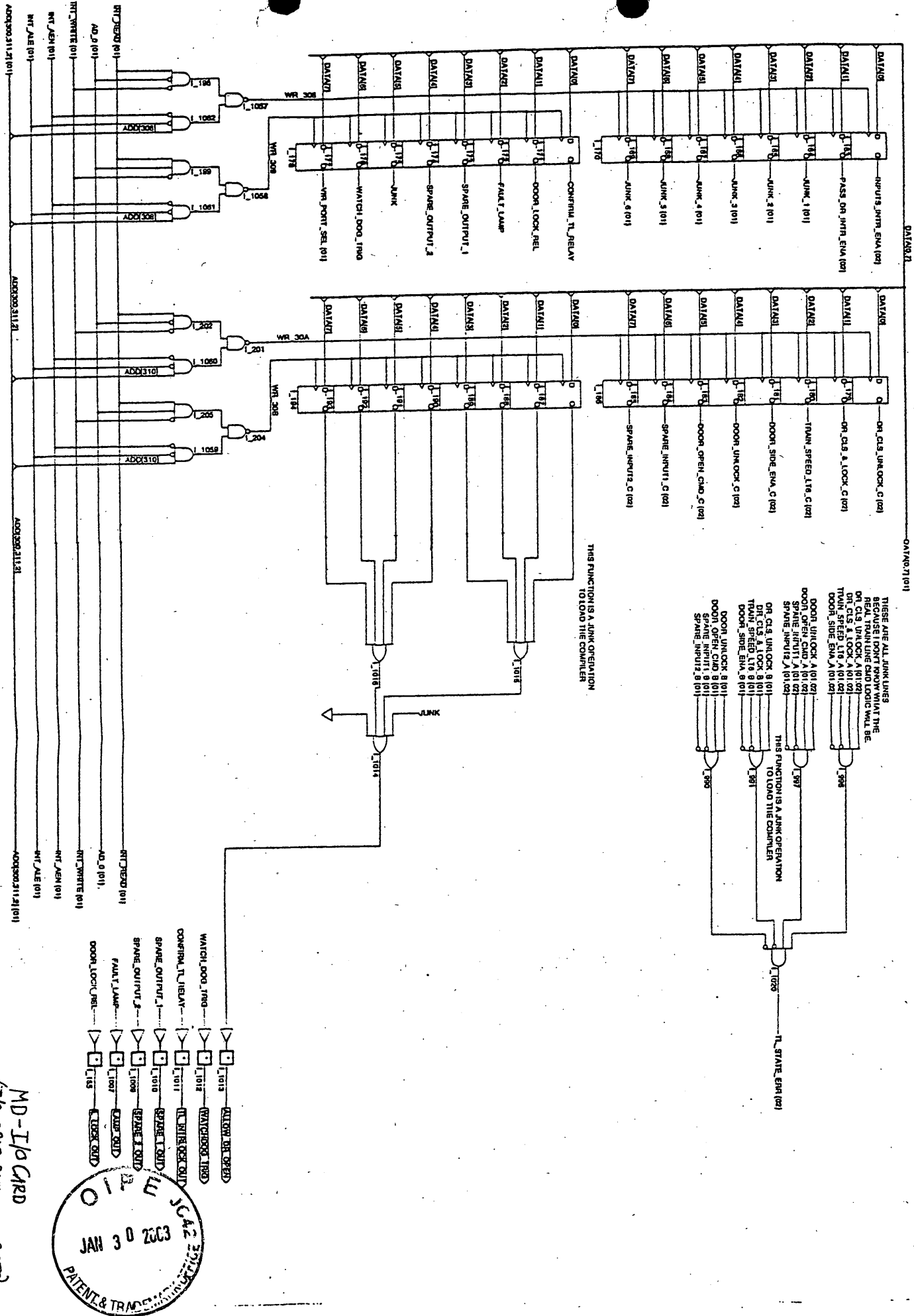
I/O-CPLD DATA/ADDRESS
CONTROL LOGIC

PATM9.71



MD-I/O CARD
(I/O-CPLD DATA WRITE PORTS)

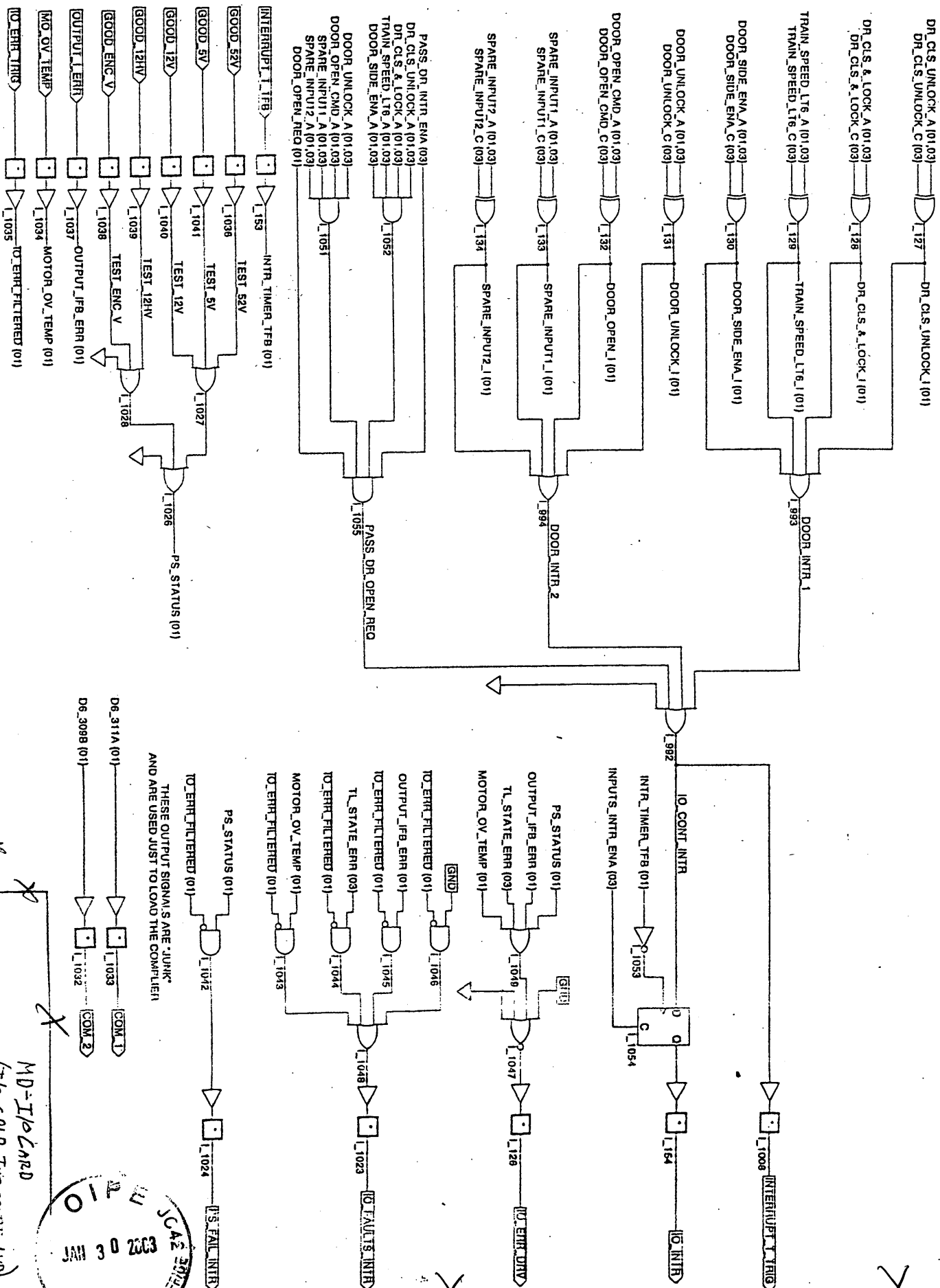
FIGURE 10 B



MD-I/O CARD
(I/O-CARD DATA WRITE PARTS)

FIGURE 78C

INTERRUPT AND FILTER CONTROL CIRCUITS



THESE OUTPUT SIGNALS ARE "JUNK" AND ARE USED JUST TO LOAD THE COMPLETION

MD-I/O CARD
(I/O-CPLD INTERRUPT AND
FILTER CONTROL CIRCUITS)

OIPF
 JAN 30 2003
 JCAZ 2003

FIGURE 10C
INTERRUPT AND FILTER CONTROL CIRCUITS

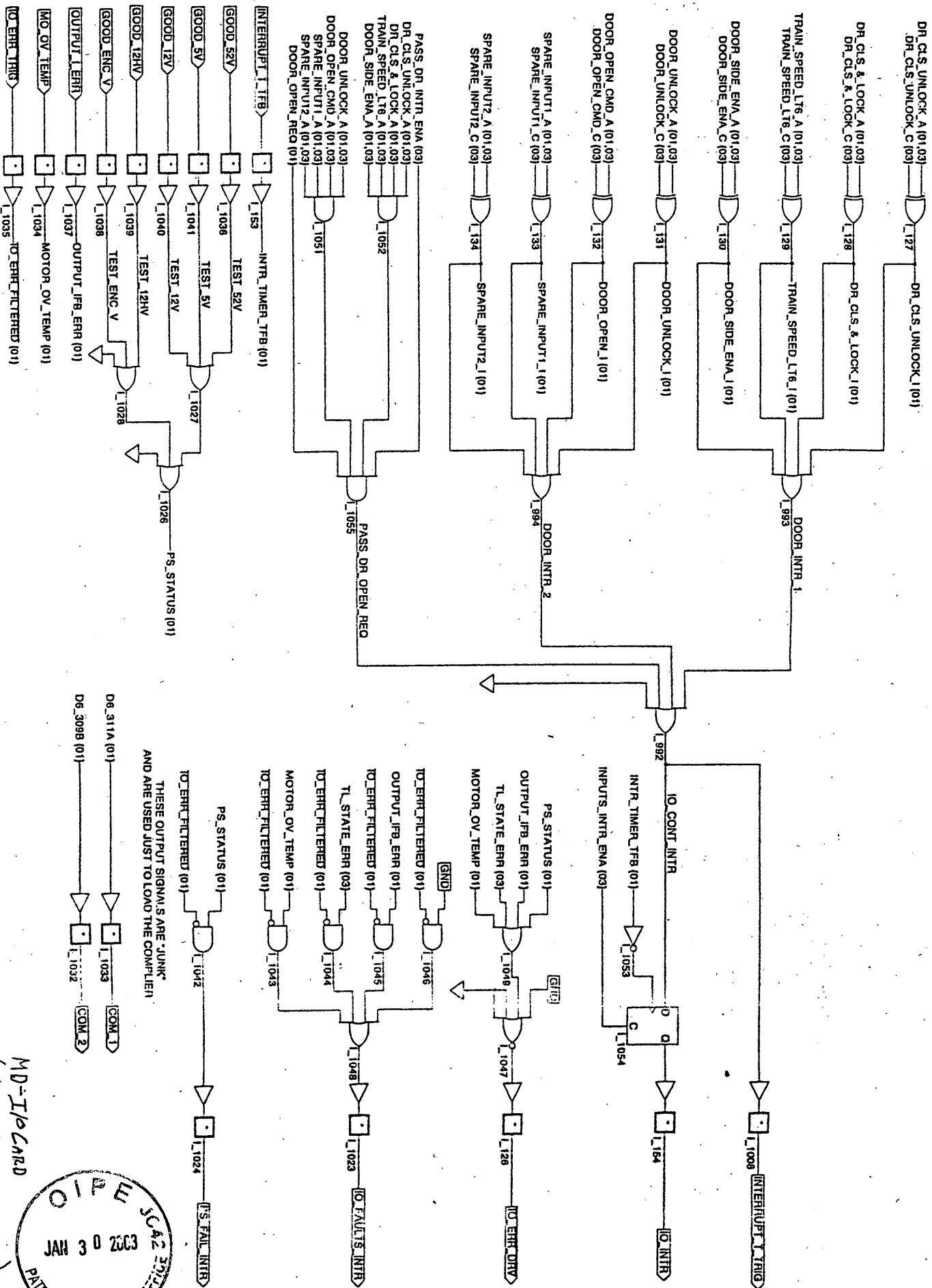
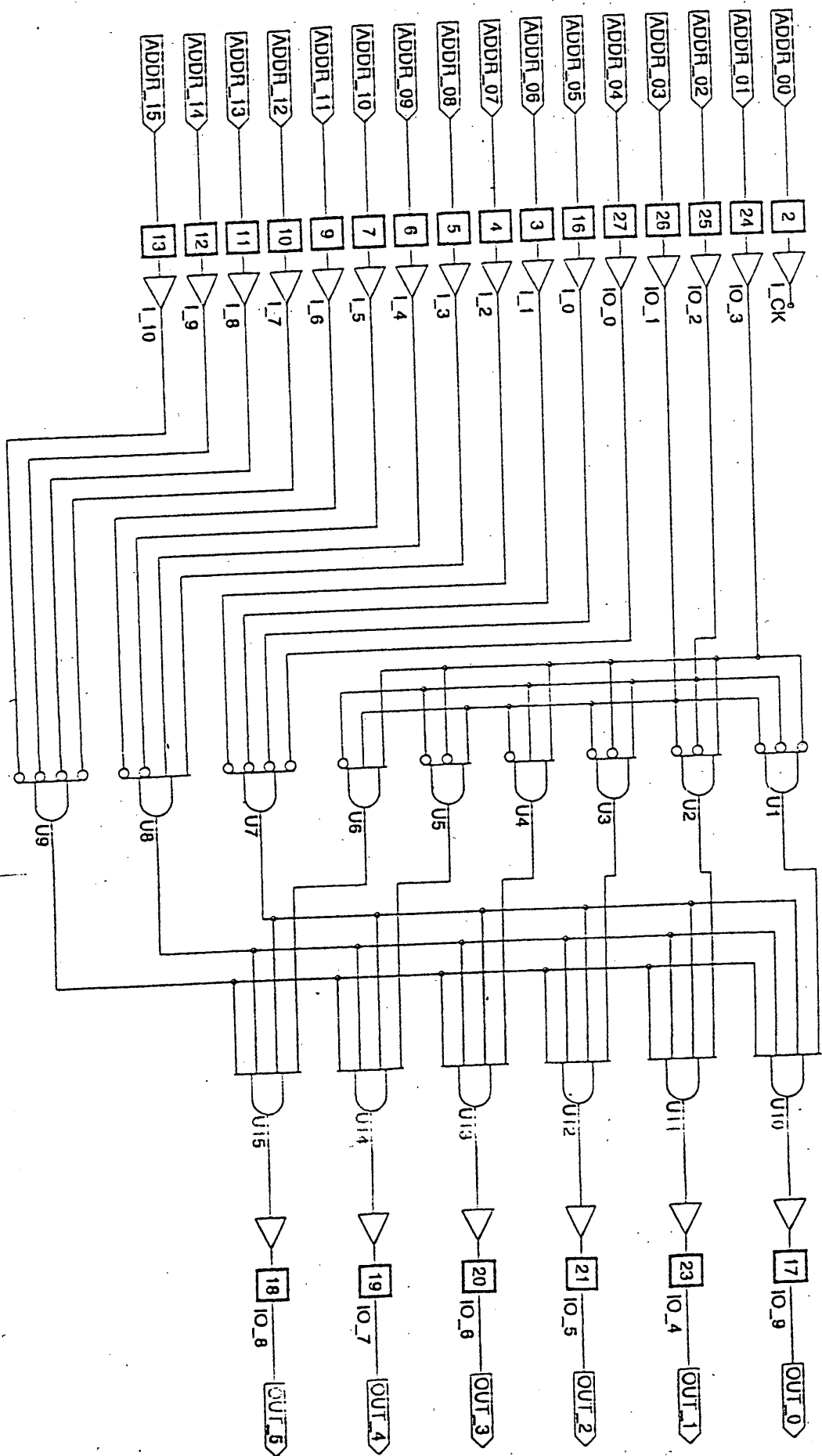


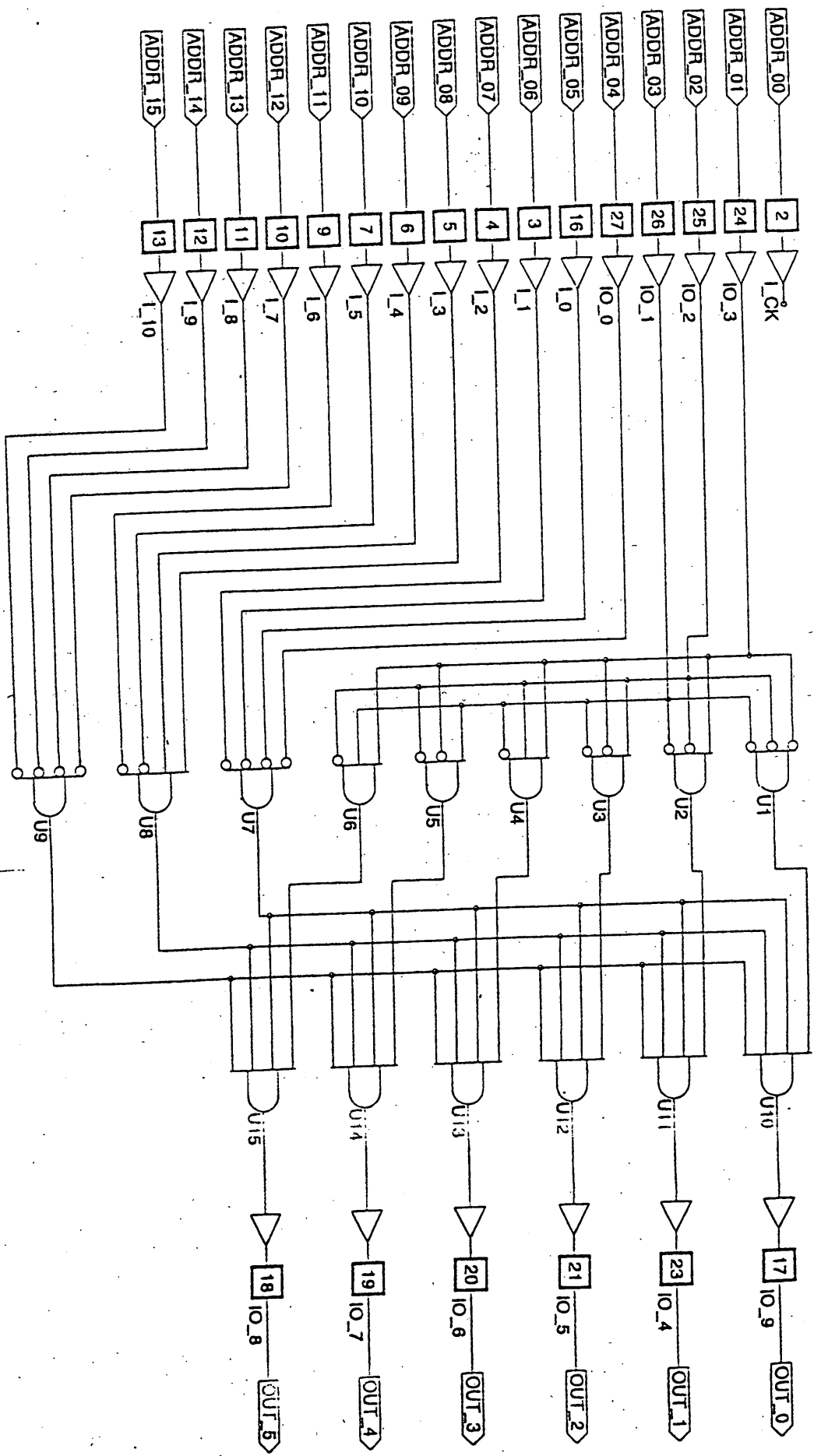
FIGURE 18



MD-I/O CARD
(ADD-CPLD LOGIC)



FIGURE 11



MD-I/O CARD
(ADD-CPLD LOGIC)



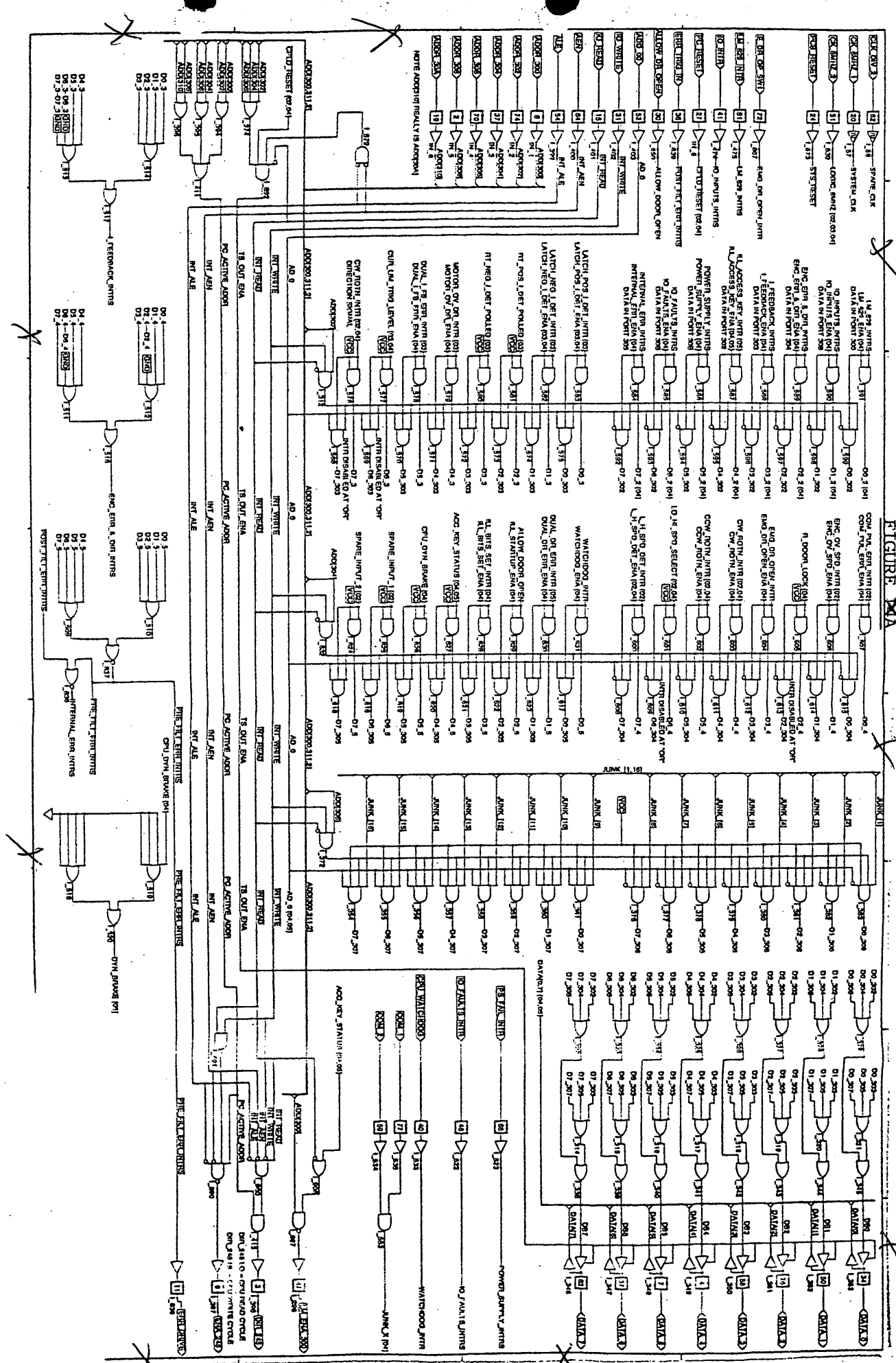
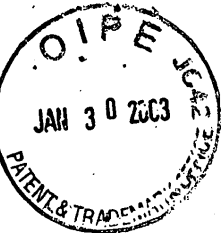
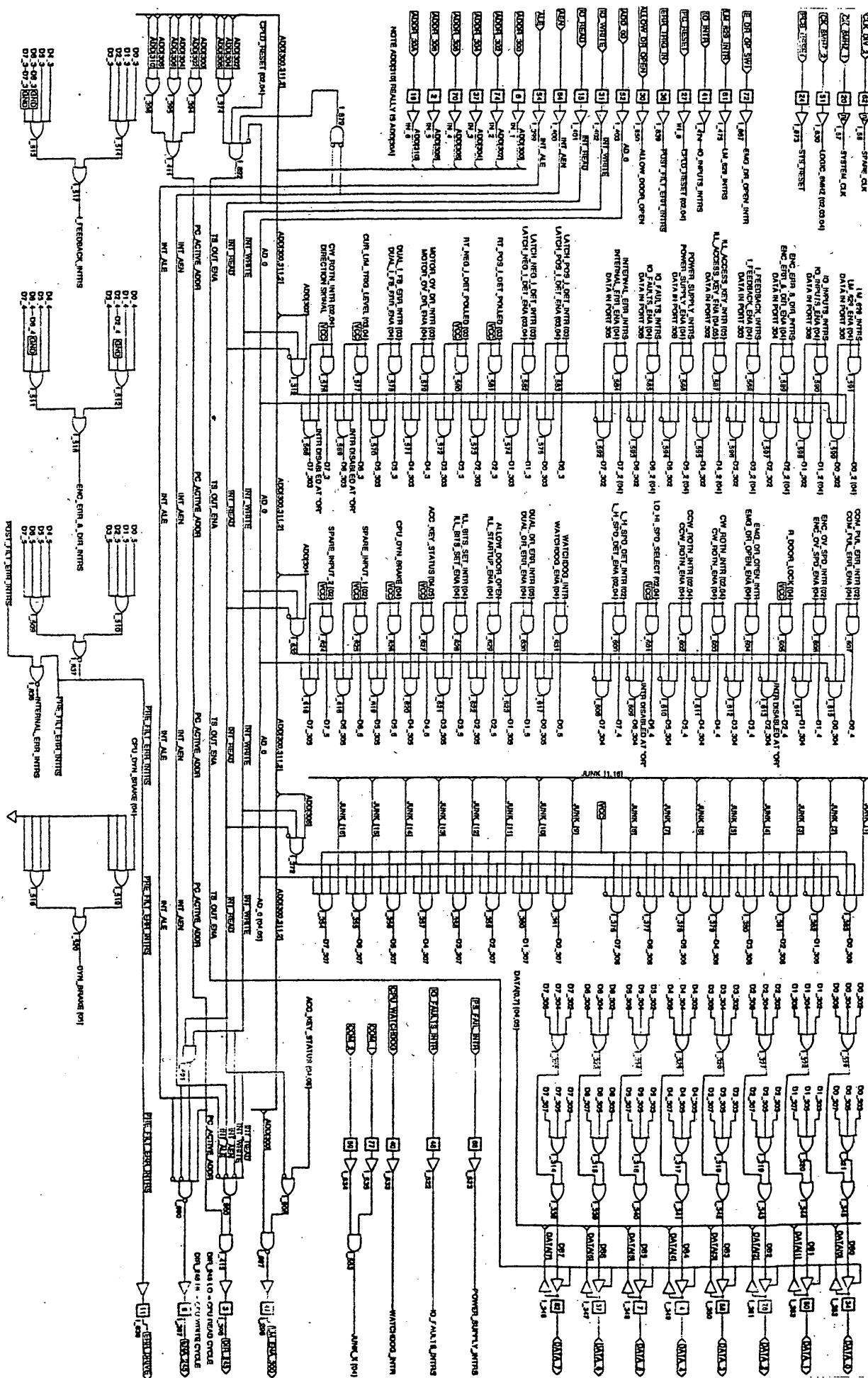


FIGURE 10A

MD-1/0 CAPD
(MC-CPLD DATA/ADDRESS)
CONTROL LOGIC

FIGURE 12A

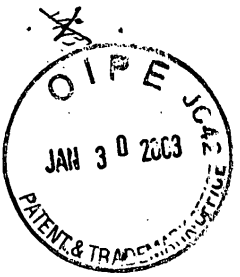
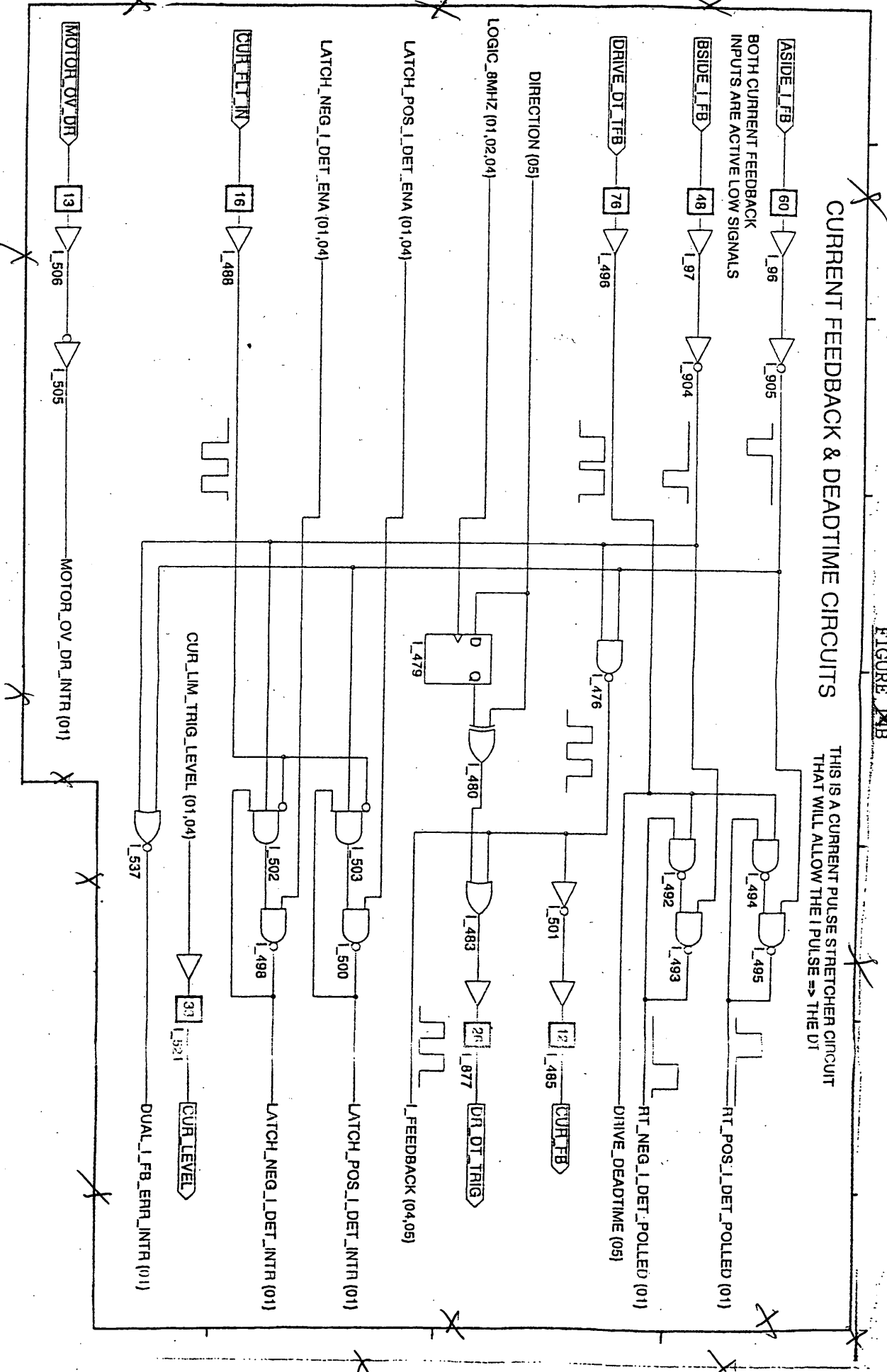


MD-1/0 CAPD
(MC-CPLD DATA/ADDRESS)
CONTROL LOGIC

FIGURE 14B

CURRENT FEEDBACK & DEADTIME CIRCUITS

THIS IS A CURRENT PULSE STRETCHER CIRCUIT THAT WILL ALLOW THE I PULSE => THE DI

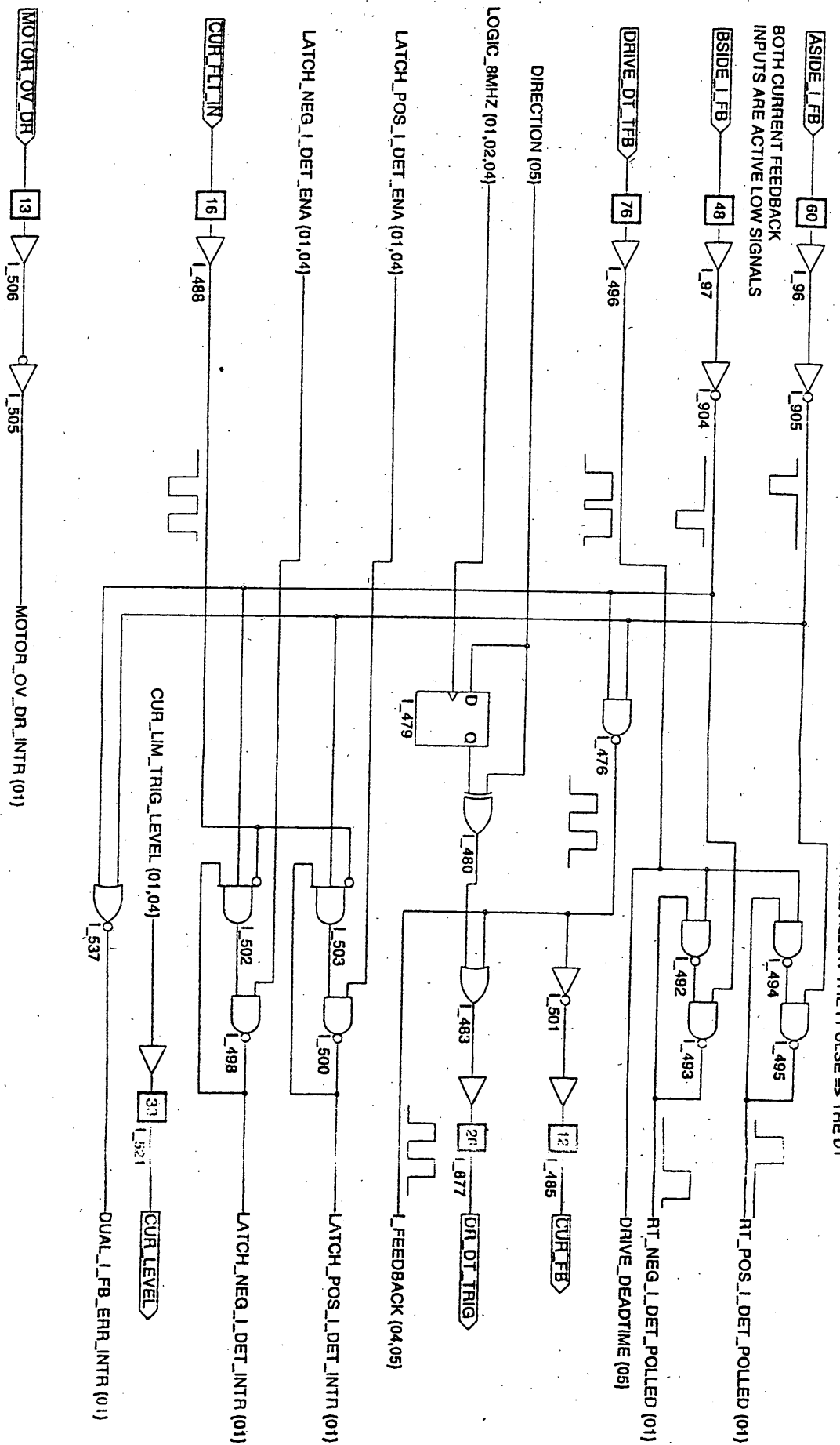


MD-I/O CARD
(MC-CPLD Current Feedback
AND DEADTIME CIRCUITS)

FIGURE 12B

CURRENT FEEDBACK & DEADTIME CIRCUITS

THIS IS A CURRENT PULSE STRETCHER CIRCUIT THAT WILL ALLOW THE I PULSE => THE DT



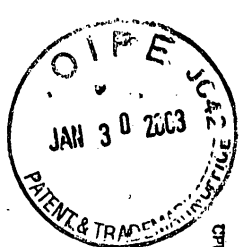
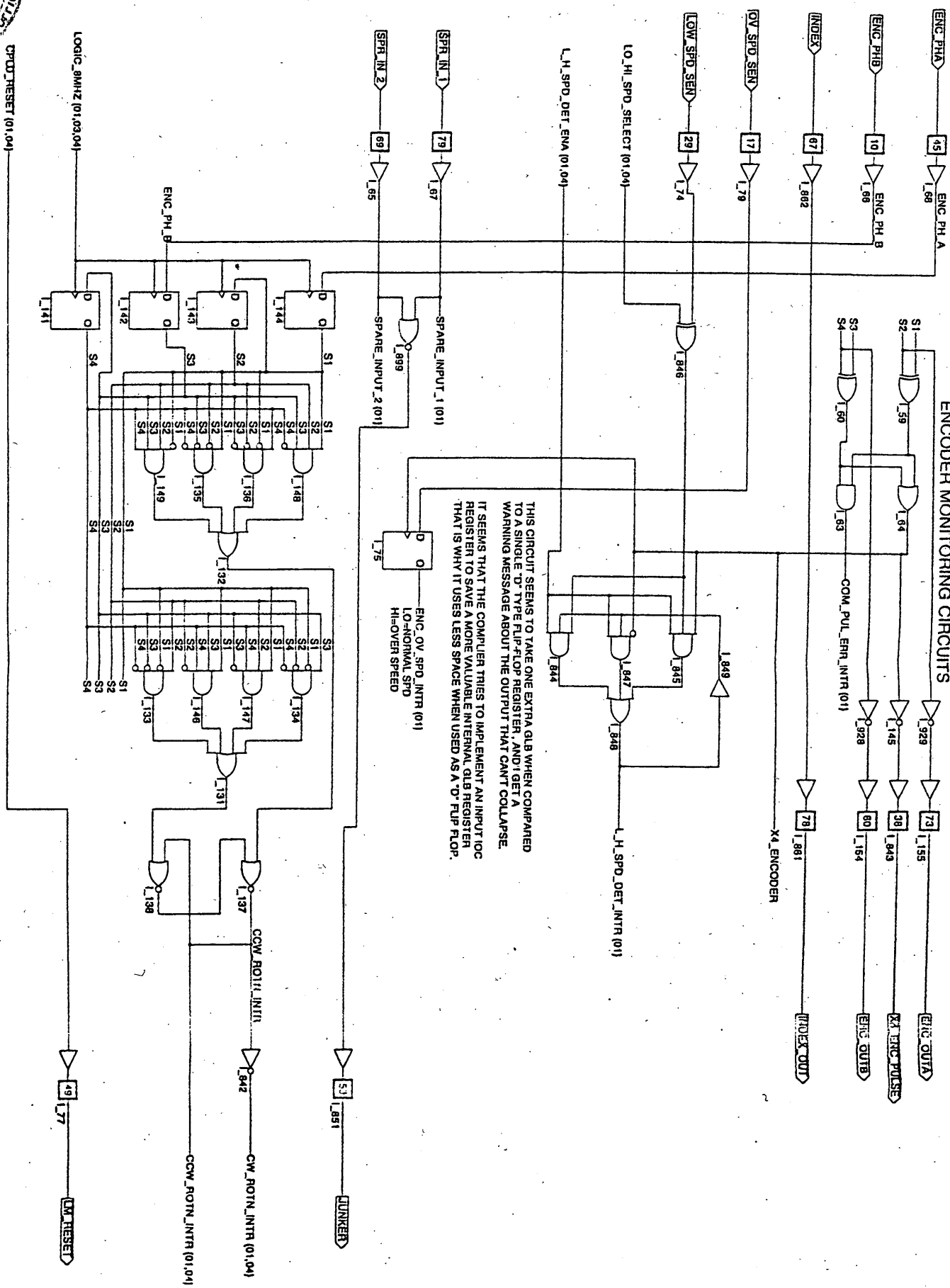
MD-I/O CARD
(MC-CPLD CURRENT FEEDBACK AND DEADTIME CIRCUITS)

ENCODER MONITORING CIRCUITS



(MC-CPLD ENCODER)
MONITORING CIRCUITS

FIGURE 12C.



MD-I/O CARD
(MC-CPLD ENCODER
Monitoring Circuits)

FIGURE 14D

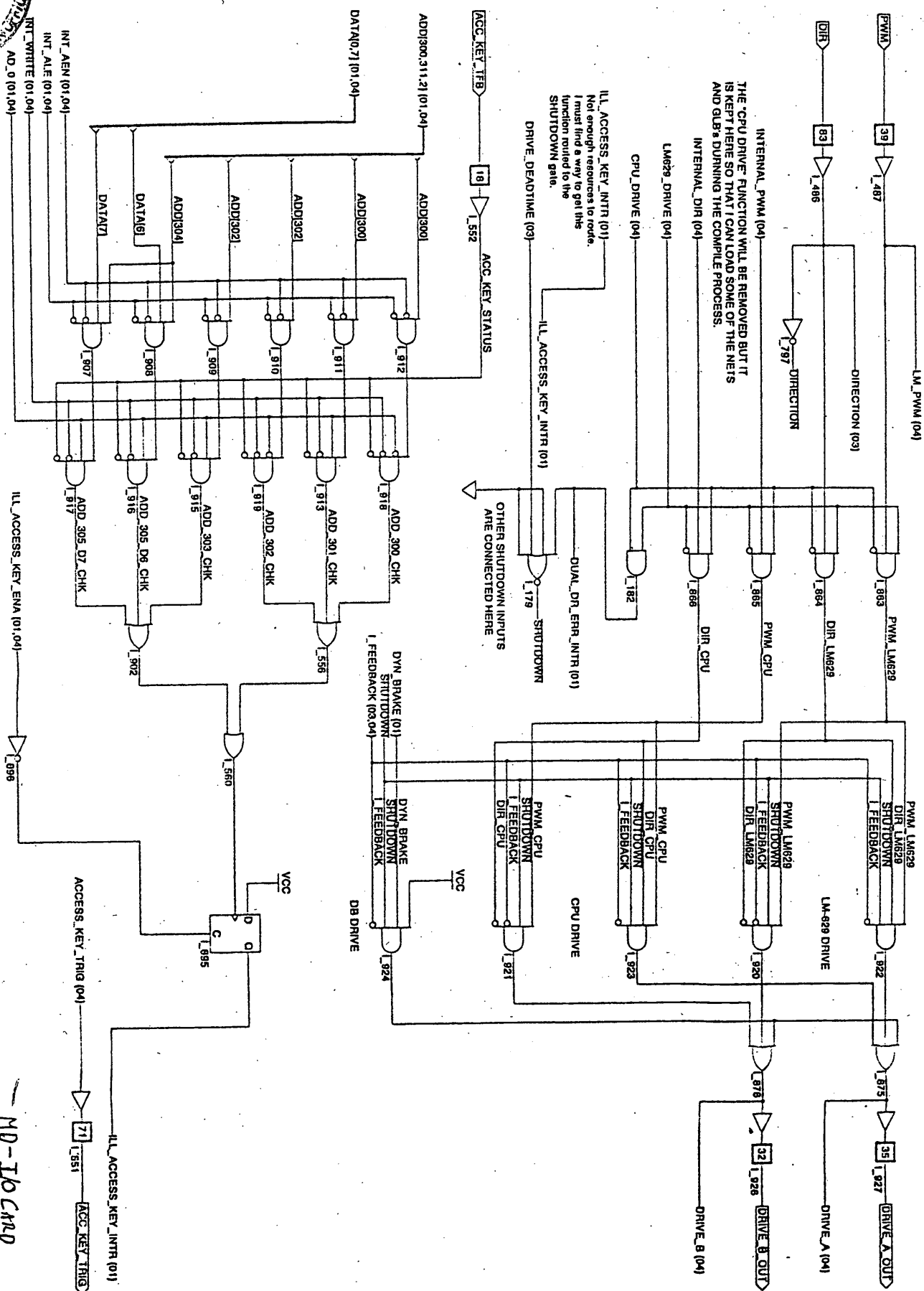


(MC-CPLD H-Bridge Control
AND Access Key Control)



FIGURE 12D

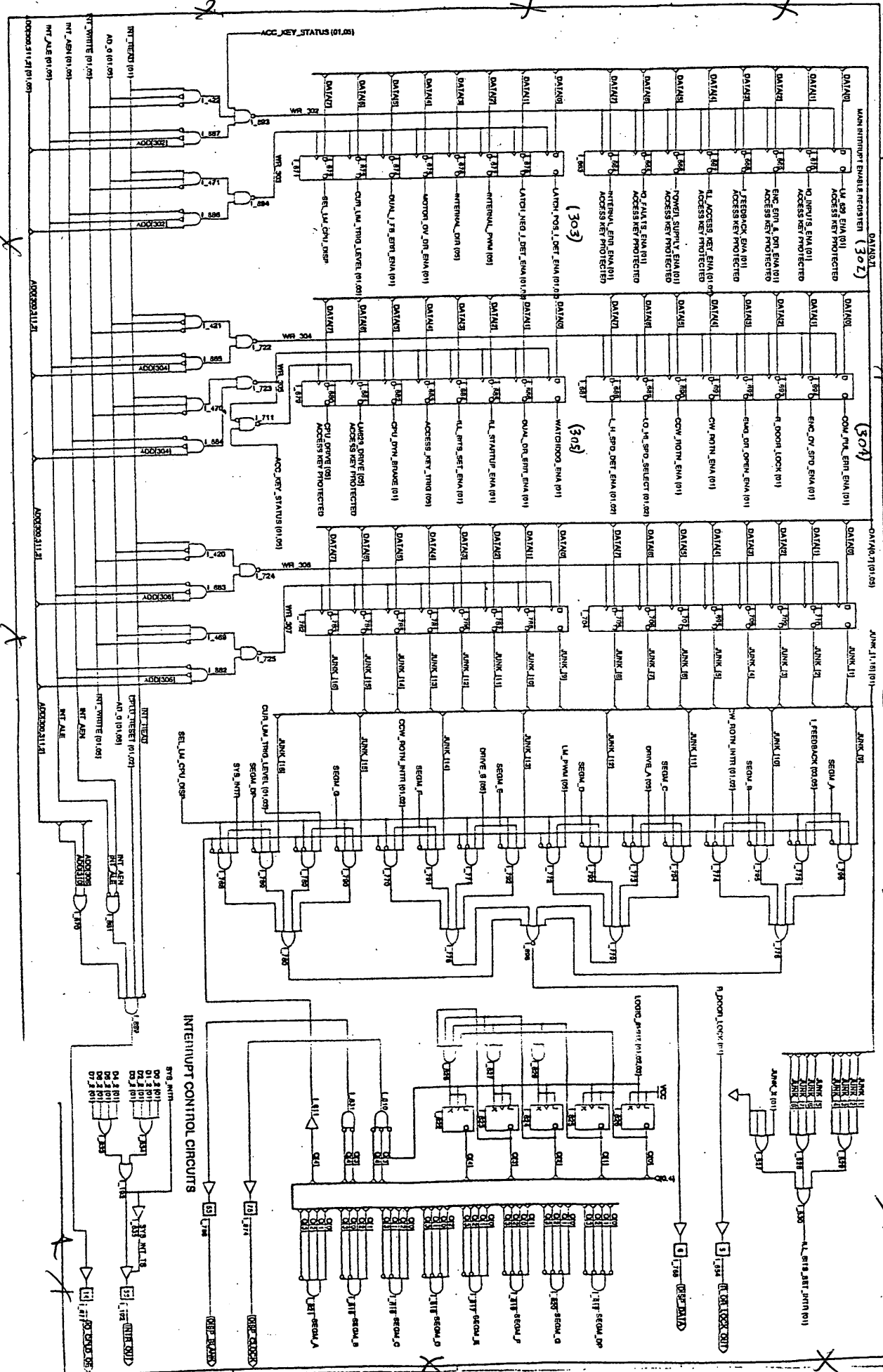
"H" BRIDGE & ACCESS KEY CONTROL CIRCUITS



MD-I/O CARD
(MC-CPLD H-BRIDGE CONTROL
AND ACCESS KEY CONTROL)

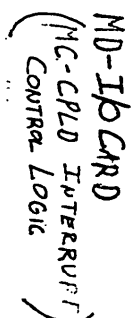


FIGURE ME



MD-1B CARD
(MC-CPLD INTERRUPT)
CONTRA LOGIC

A circular ink stamp from the U.S. Patent & Trademark Office. The date "JAN 30 2003" is stamped in the center. The words "U.S. PATENT & TRADEMARK OFFICE" are curved along the top and right edges of the circle.



(MC-CPLD INTERRUPT
CONTRA LOGIC)

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